

FIG. 1

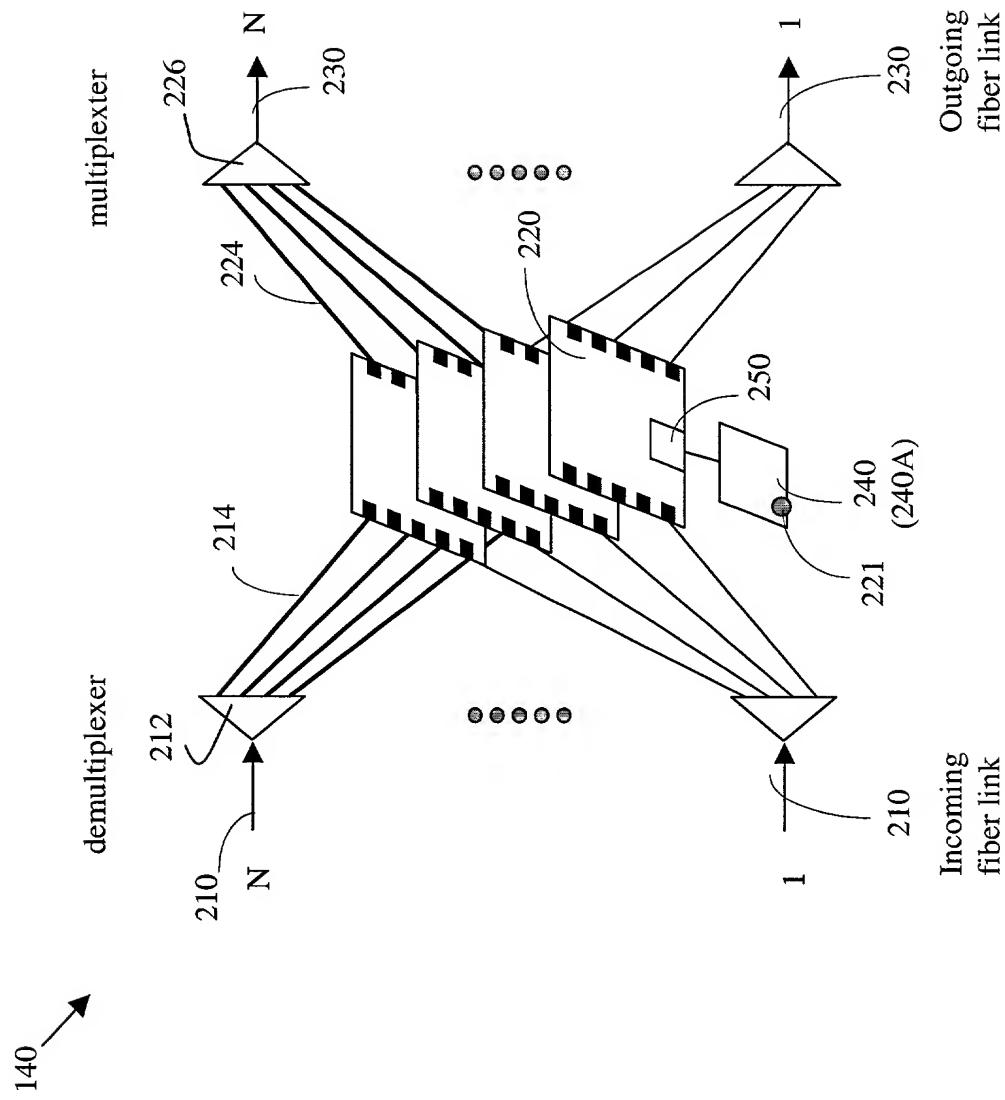


FIG. 2

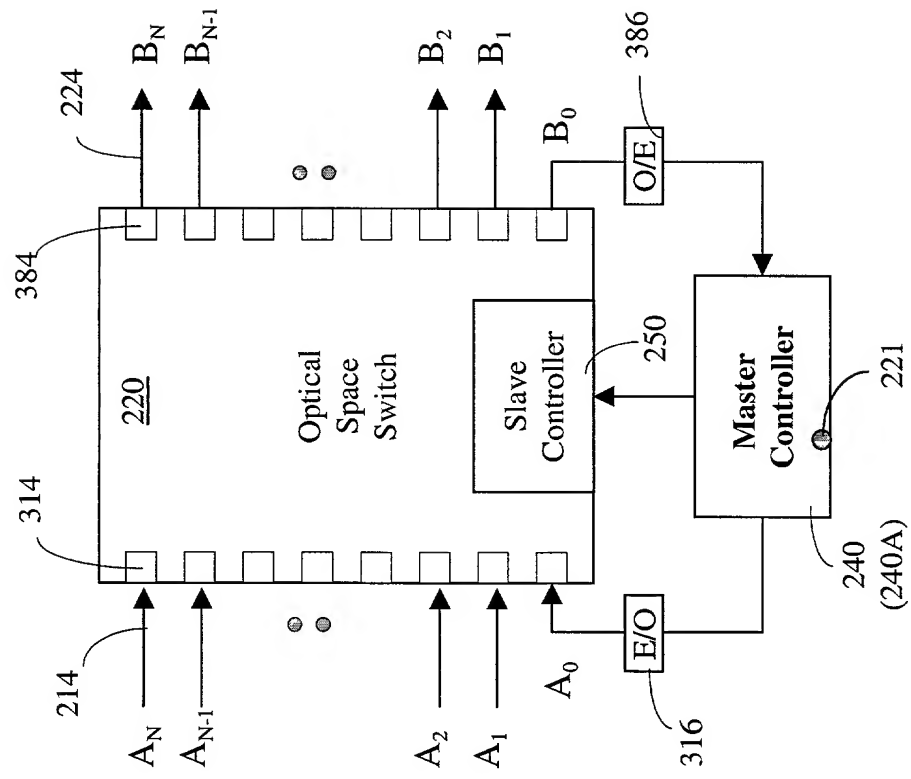


FIG. 3

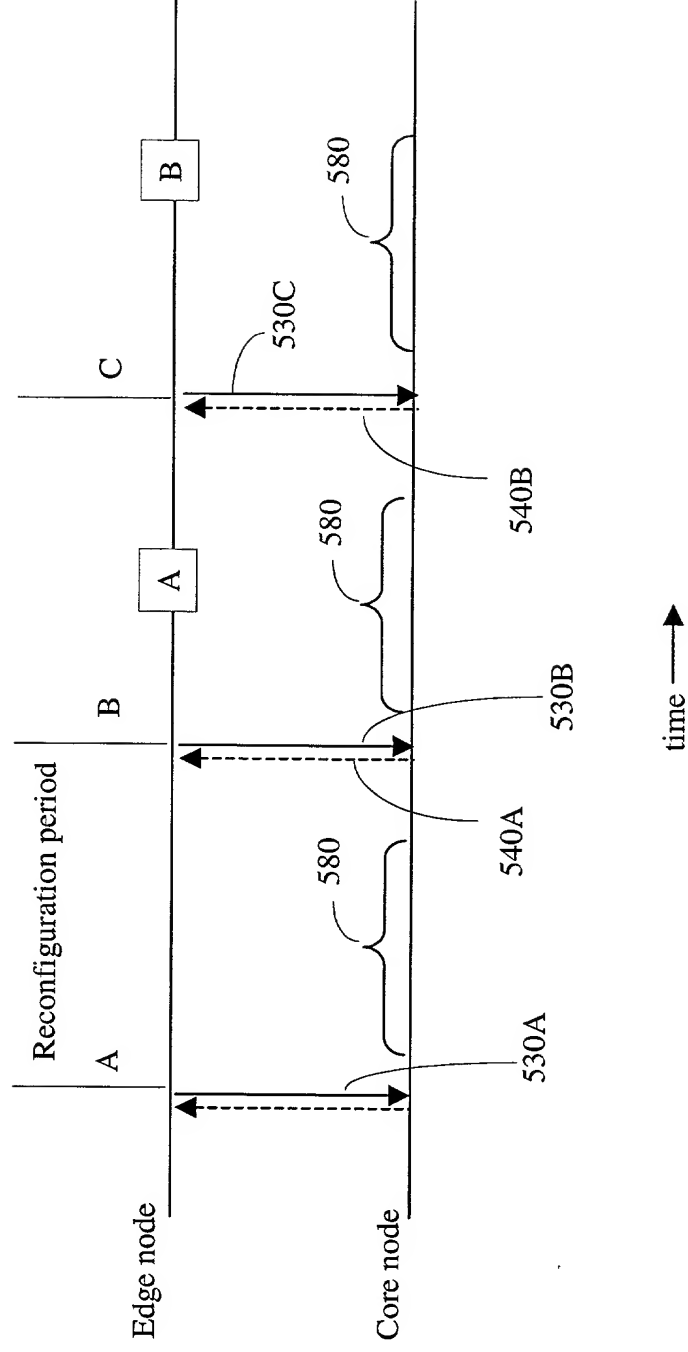


FIG. 5

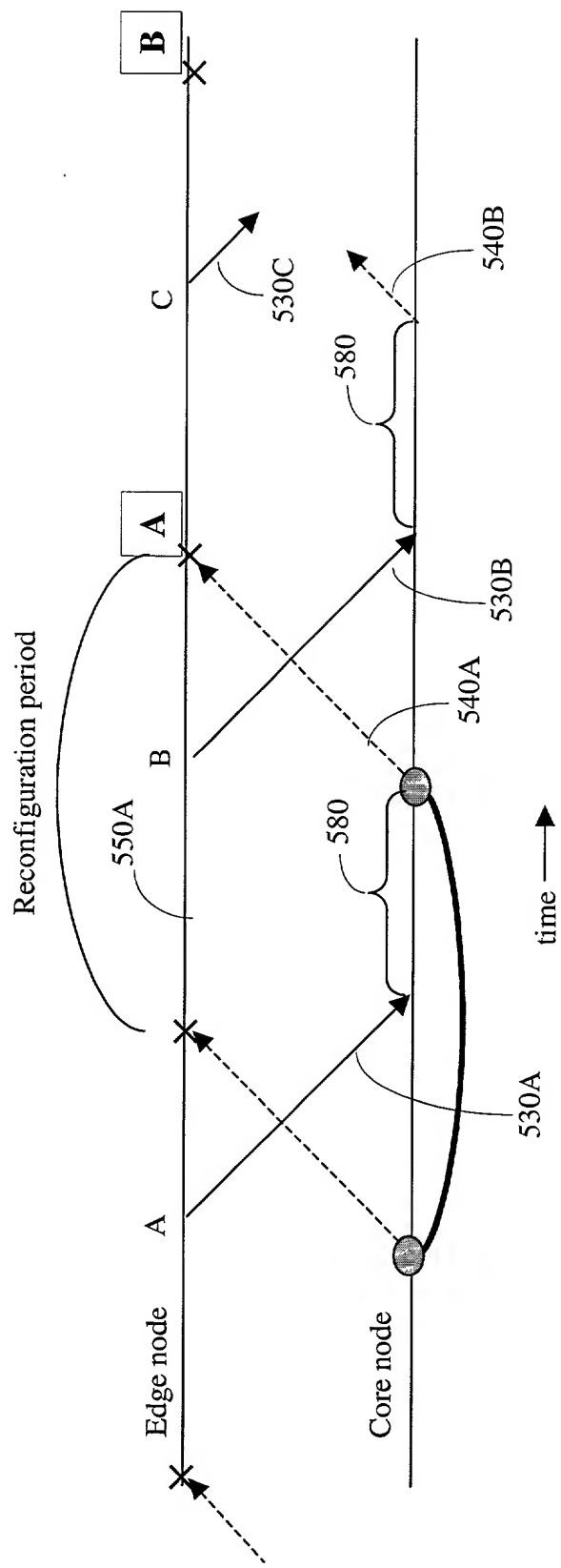


FIG. 6

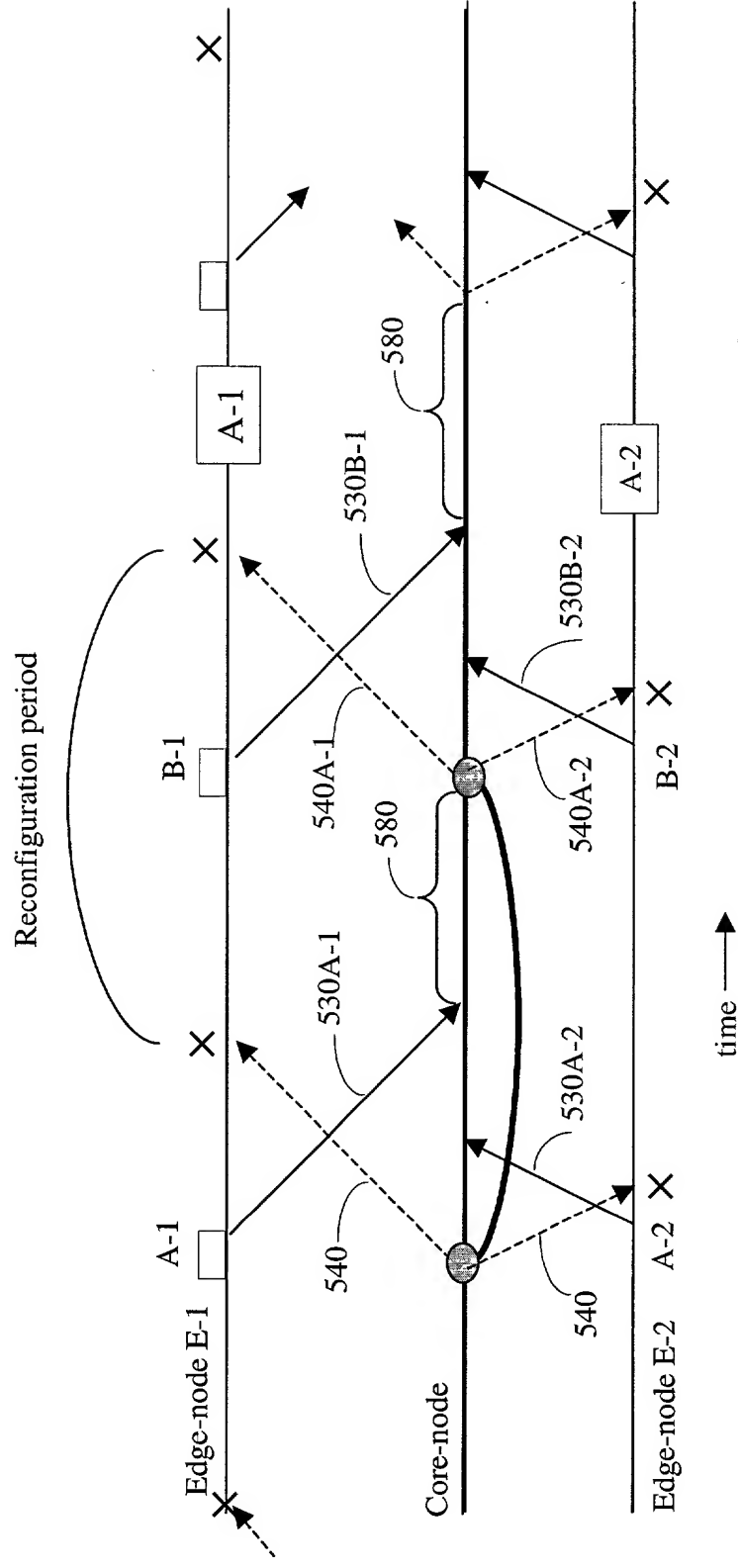


FIG. 7

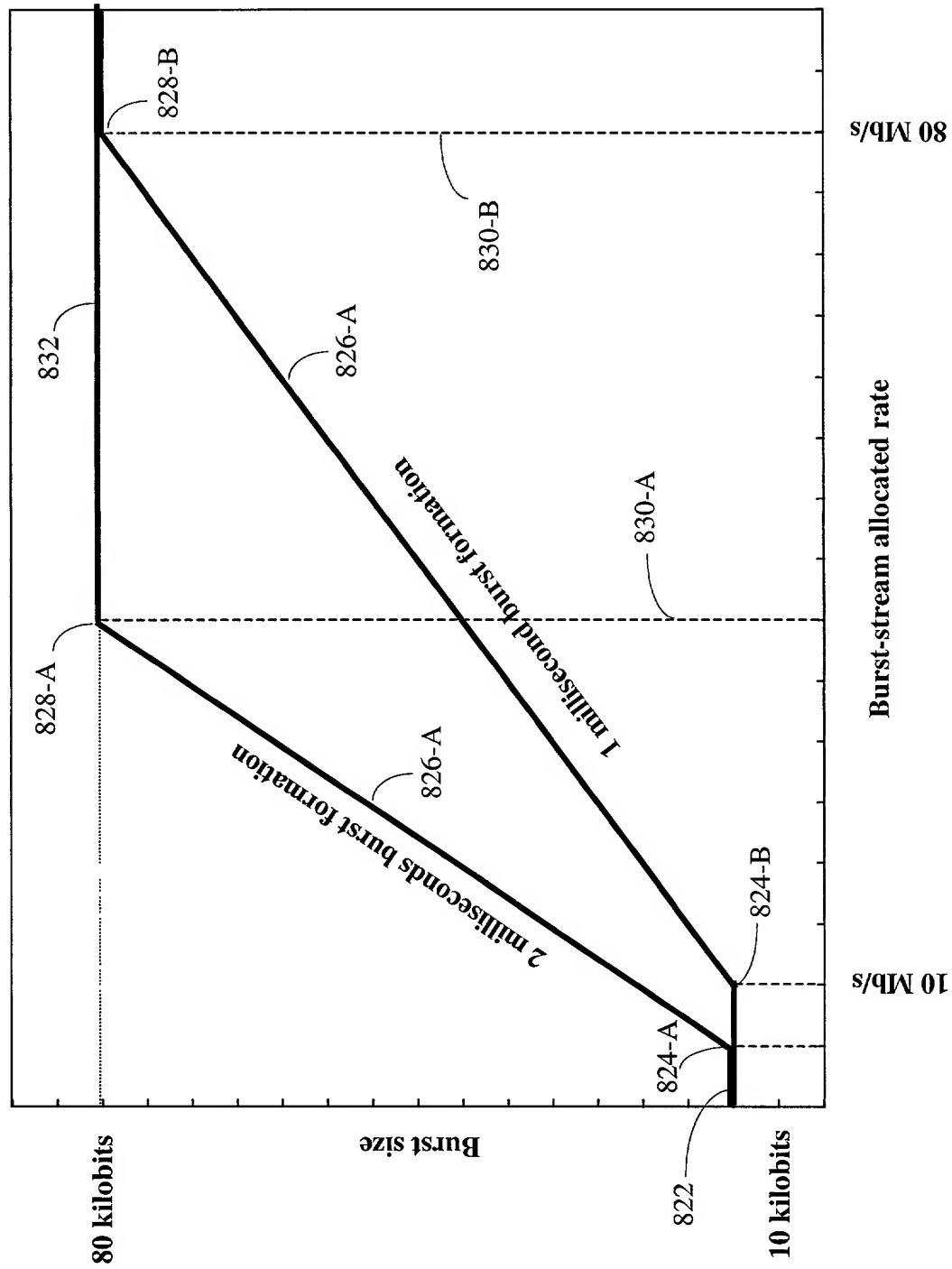


FIG. 8

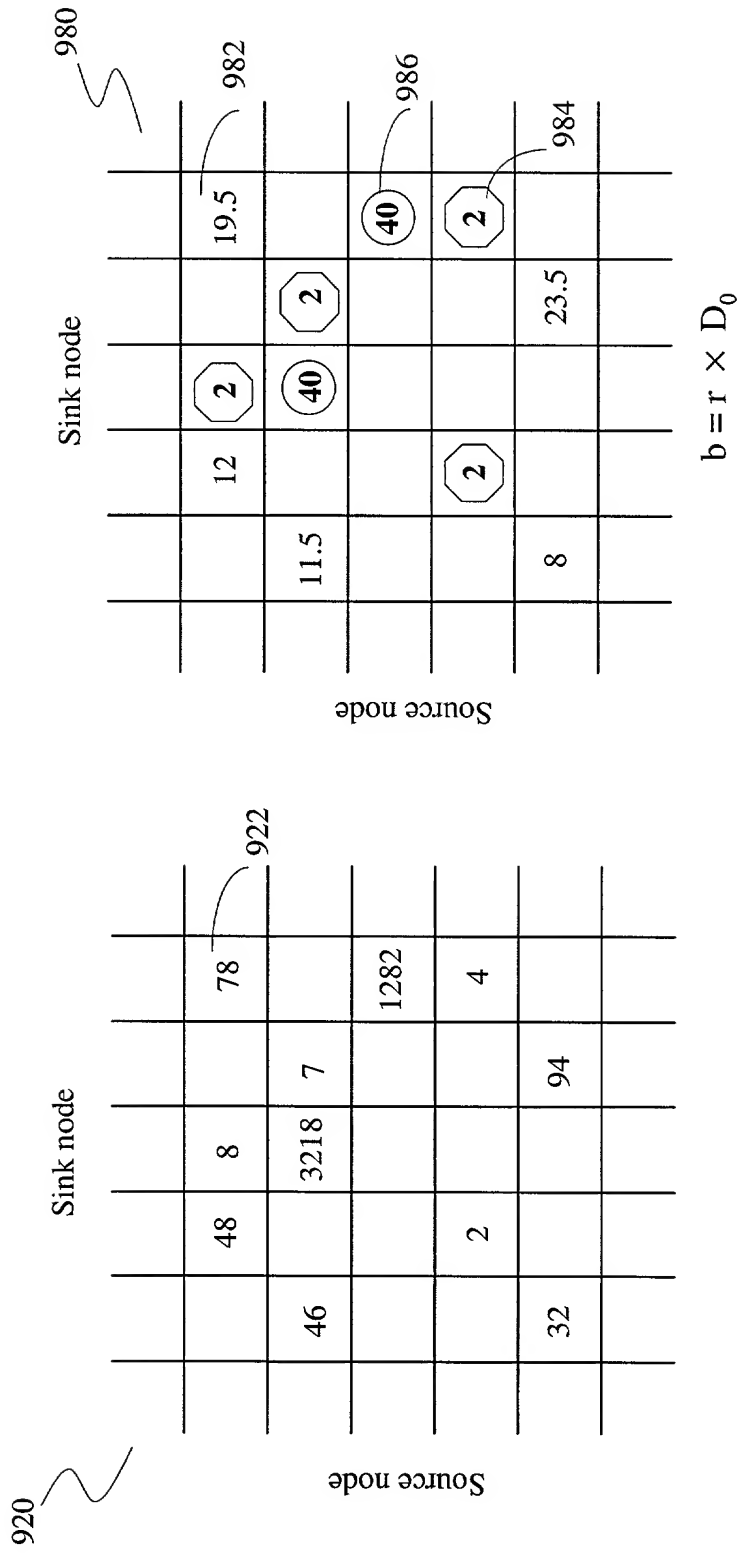


FIG. 9

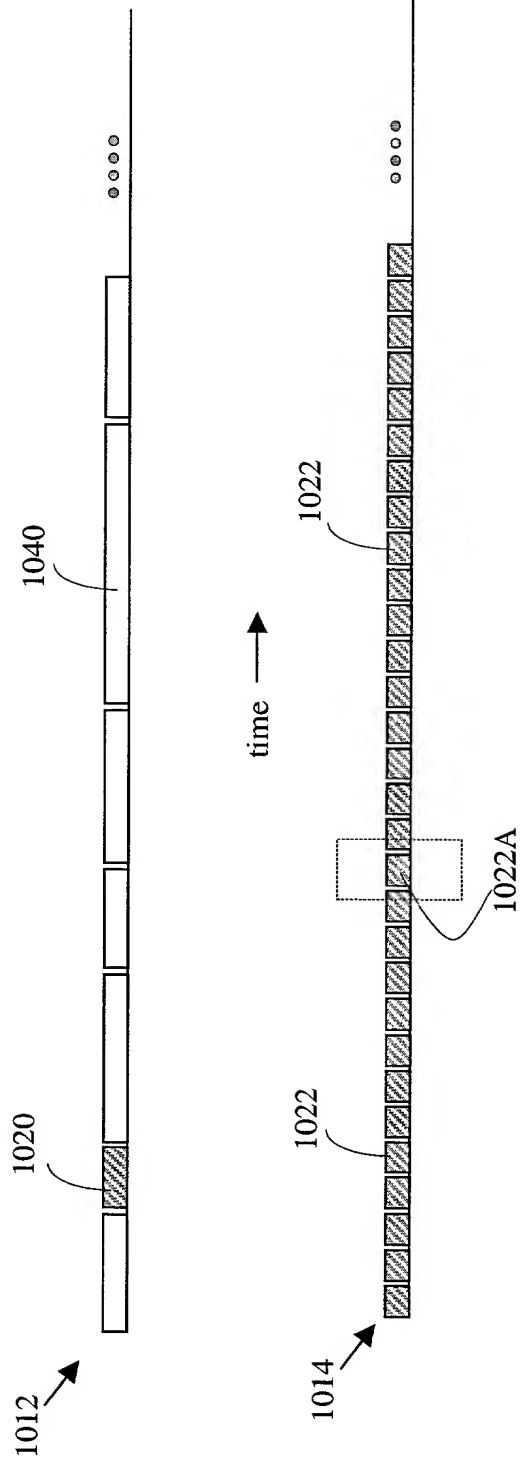


FIG. 10

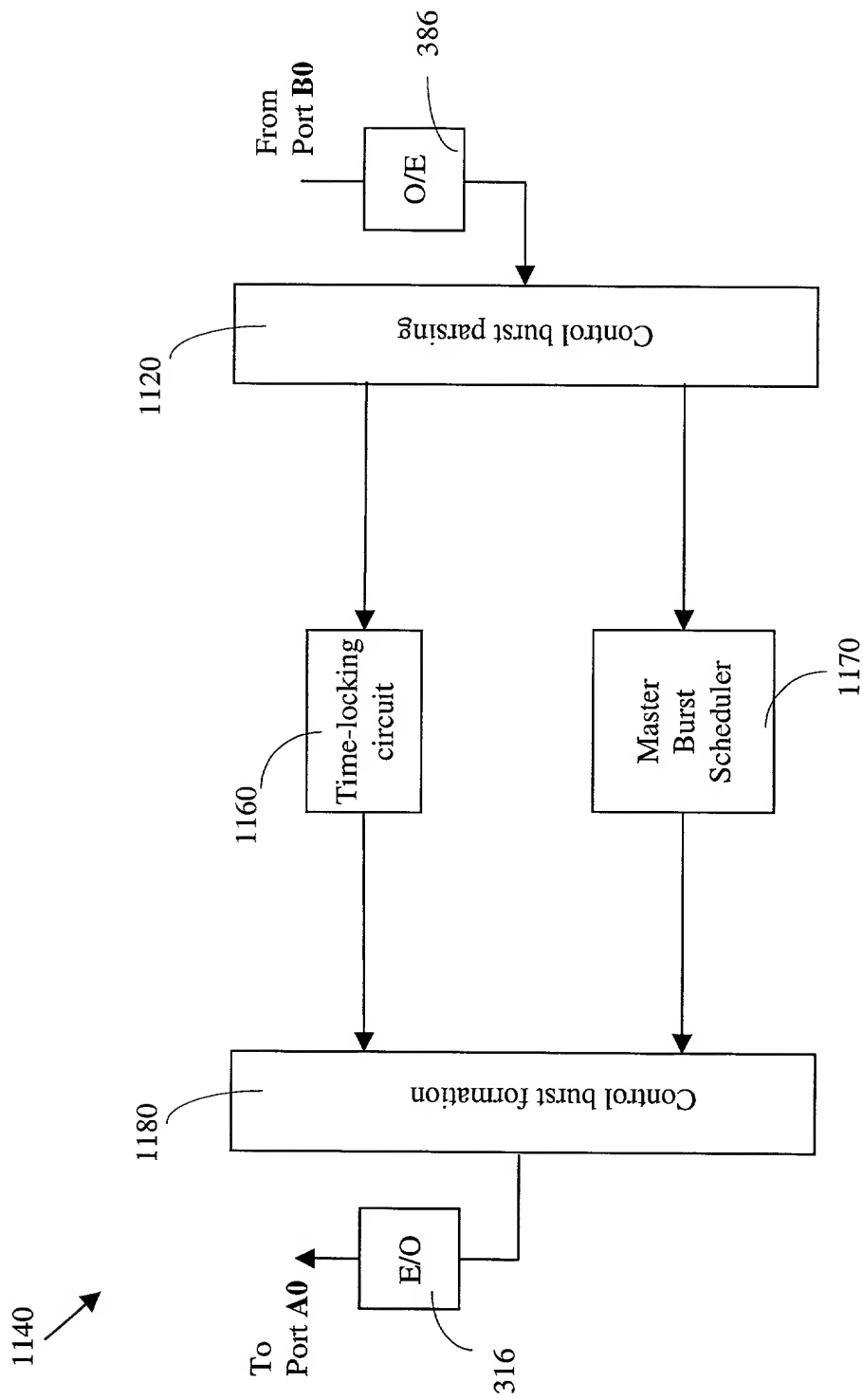


FIG. 11

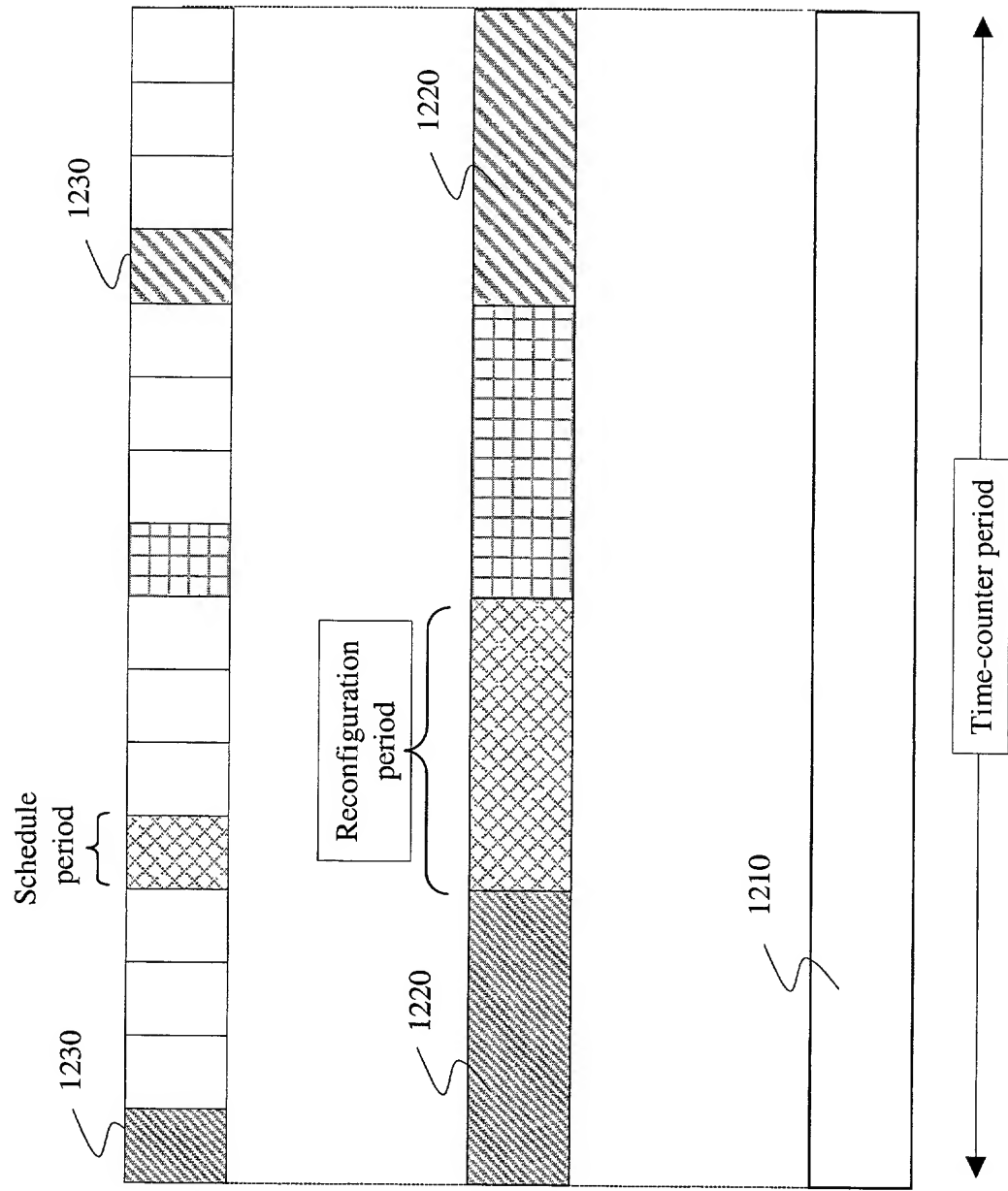


FIG. 12

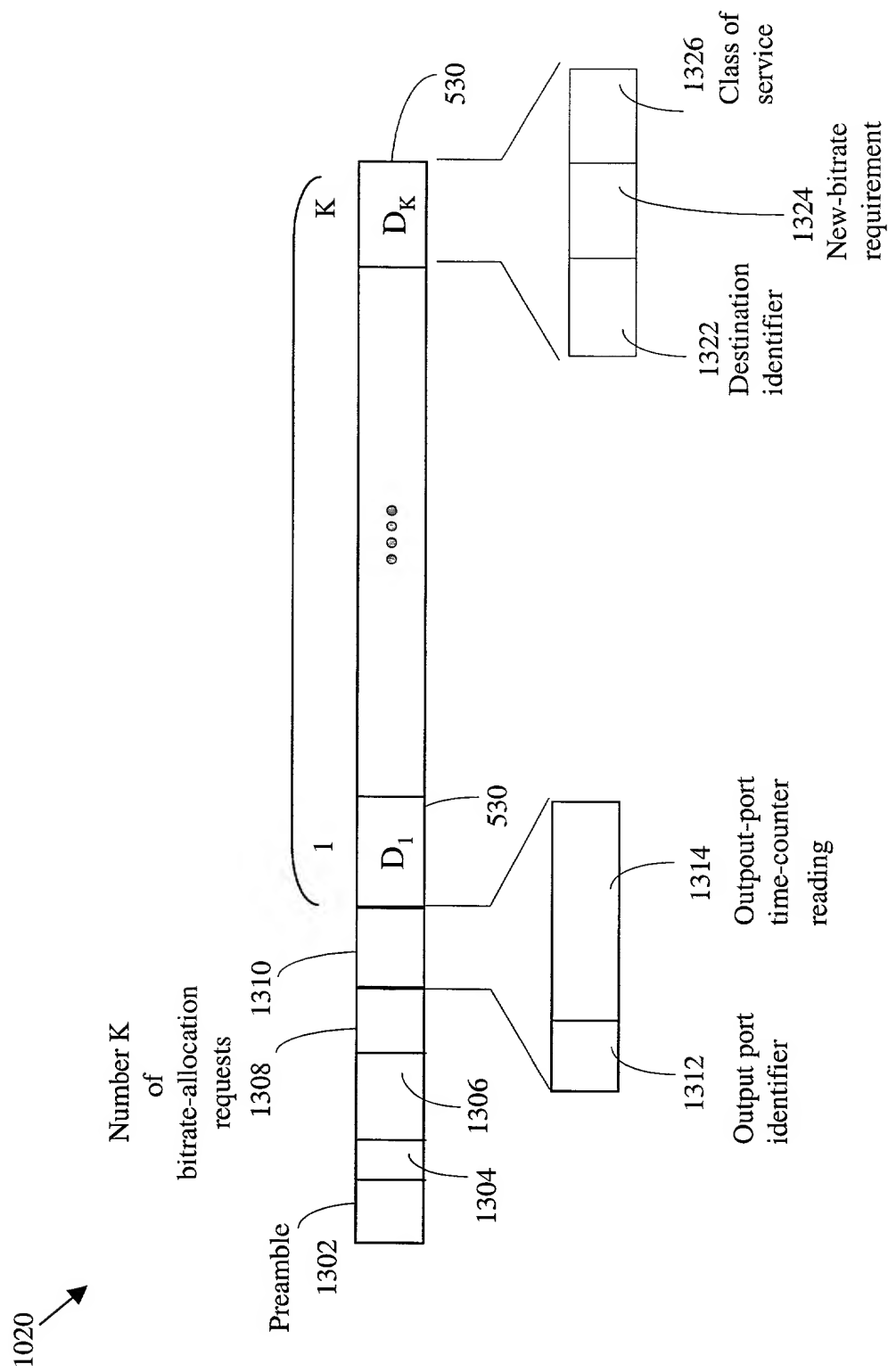


FIG. 13

1400

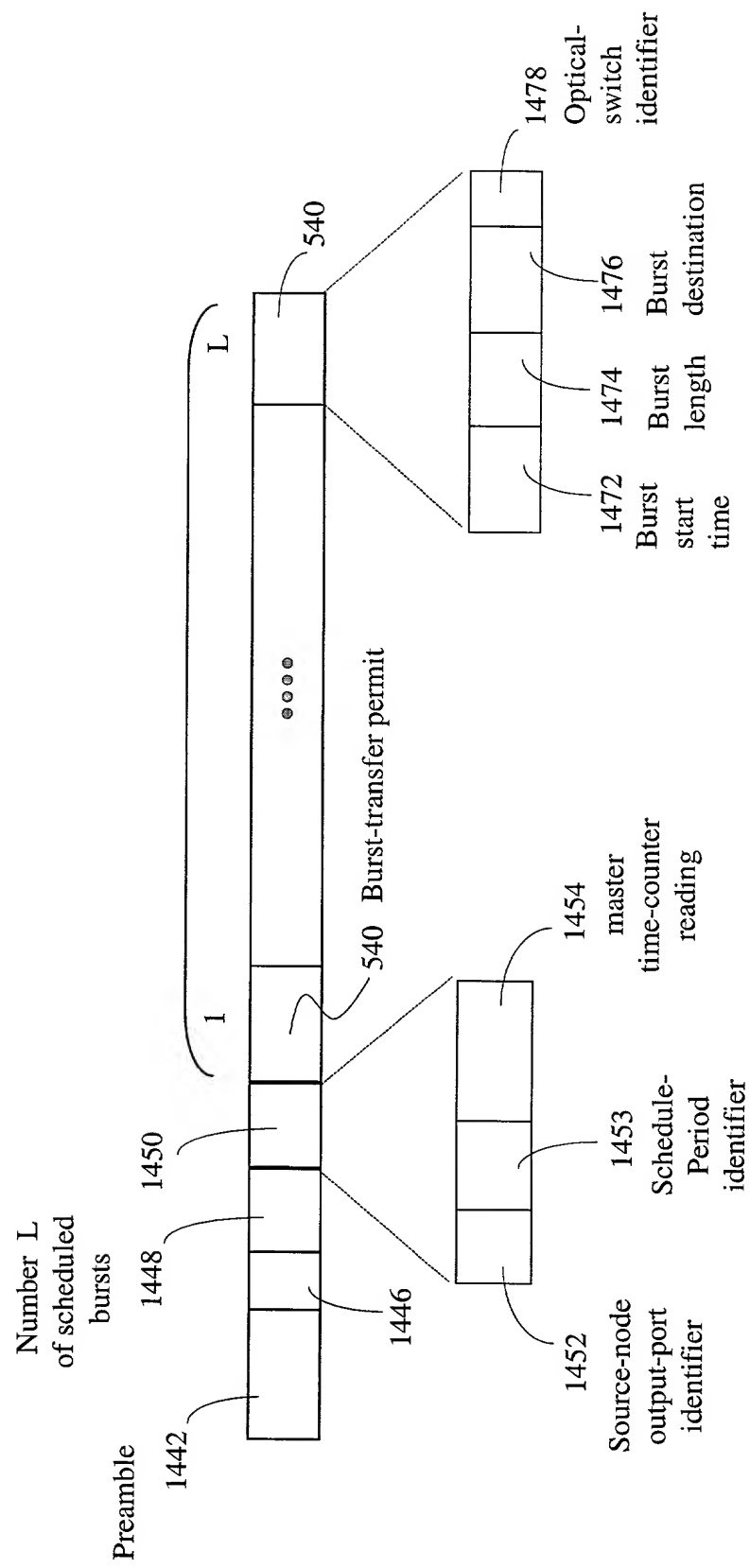


FIG. 14

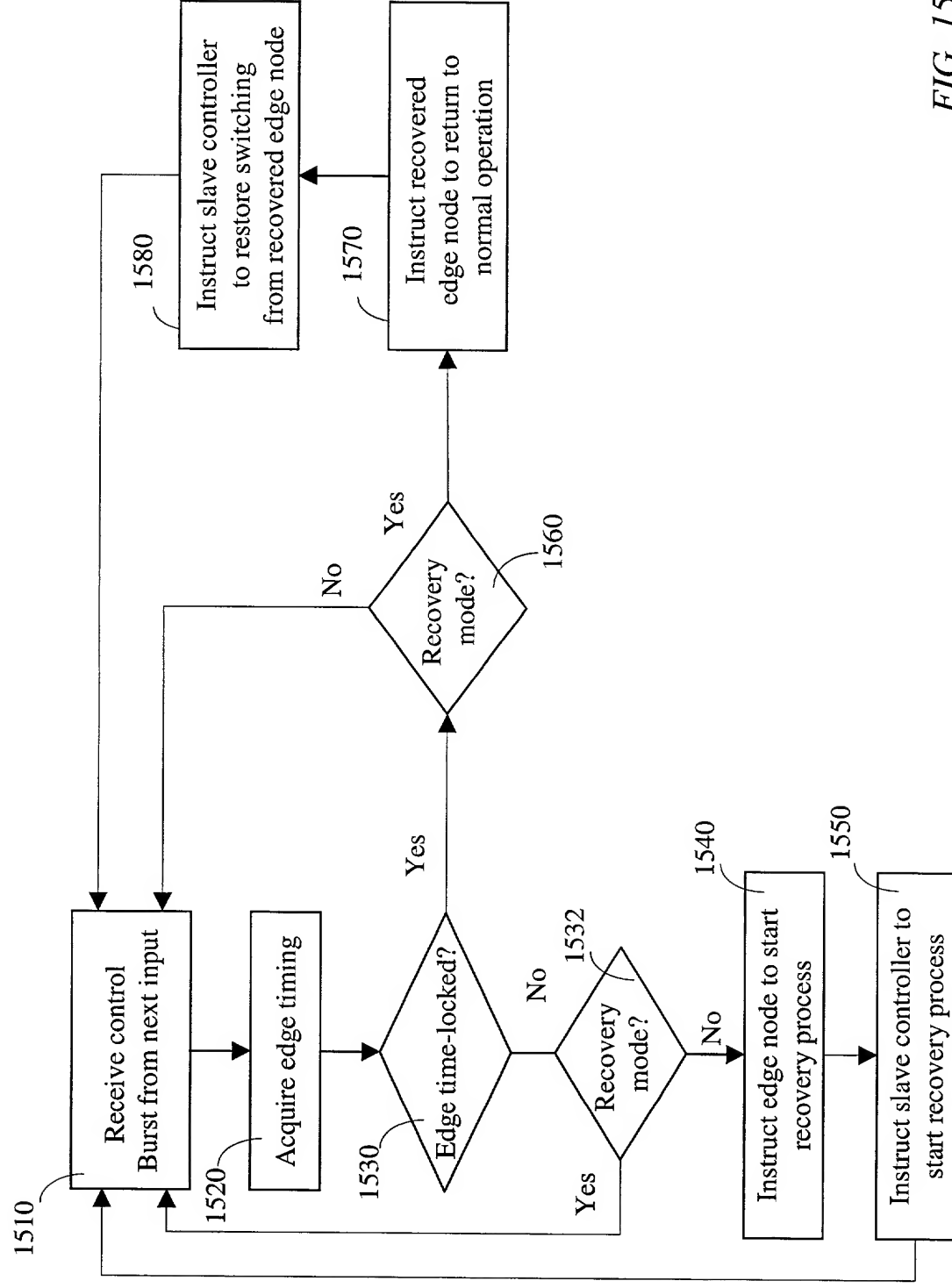


FIG. 15

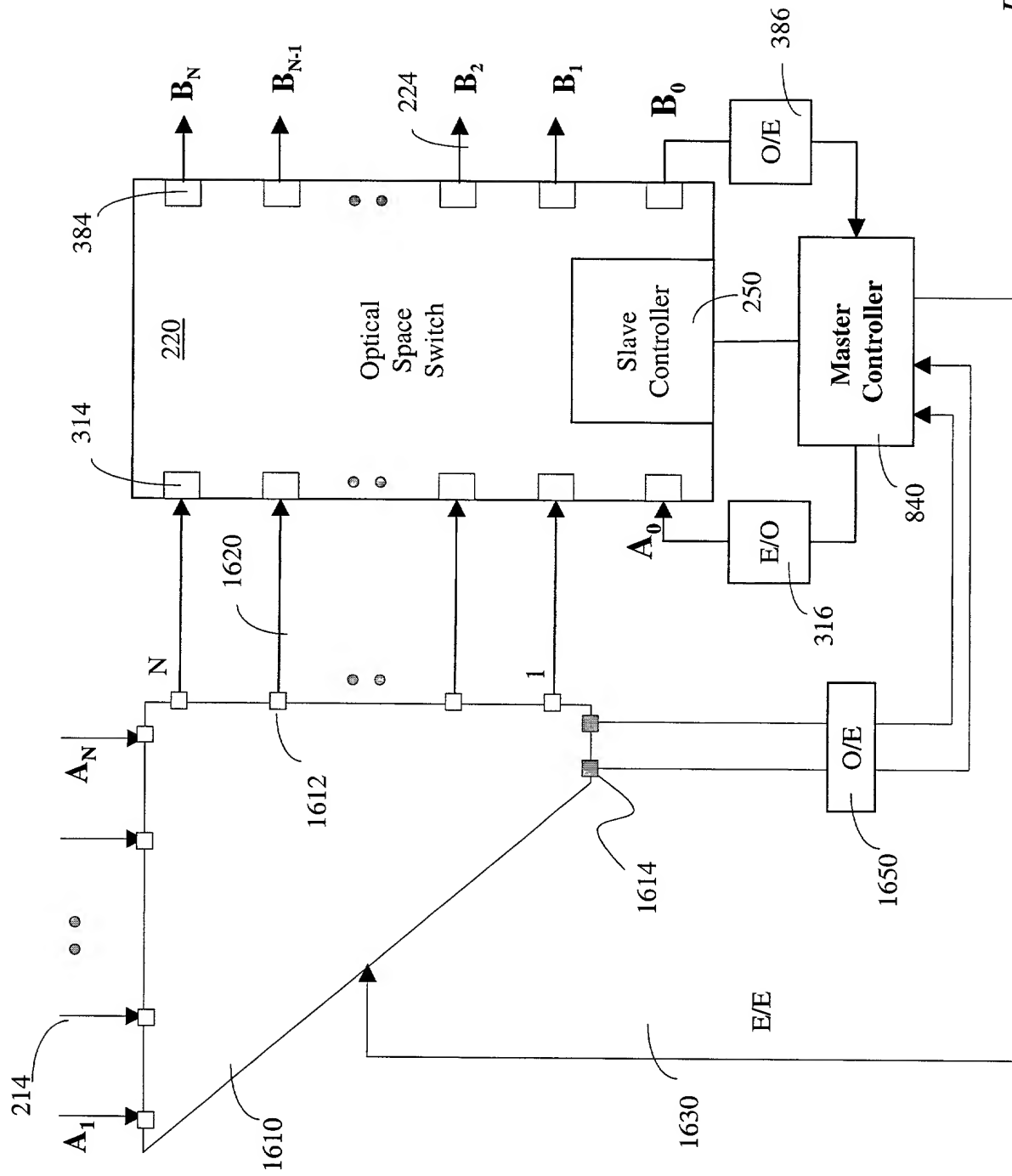


FIG. 16

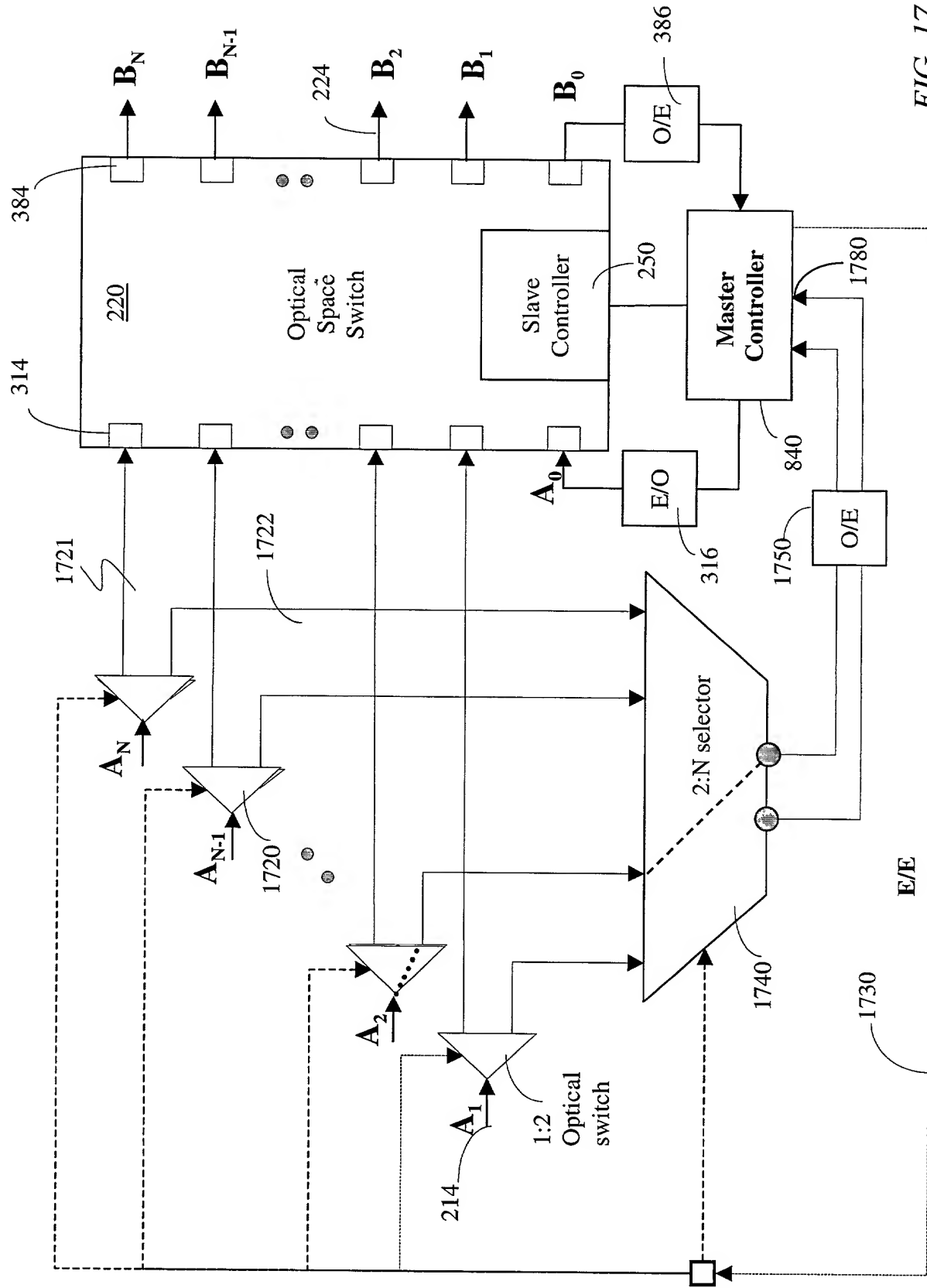


FIG. 17

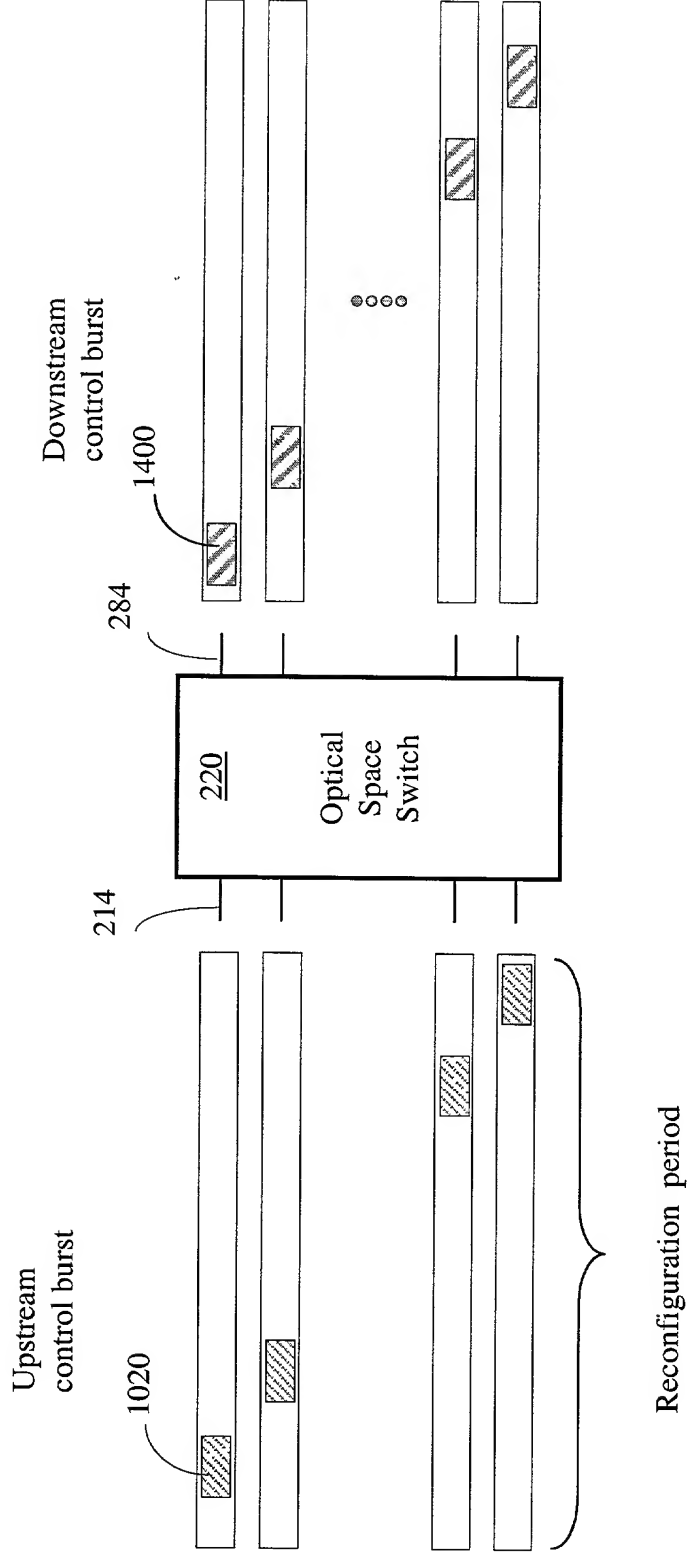


FIG. 18

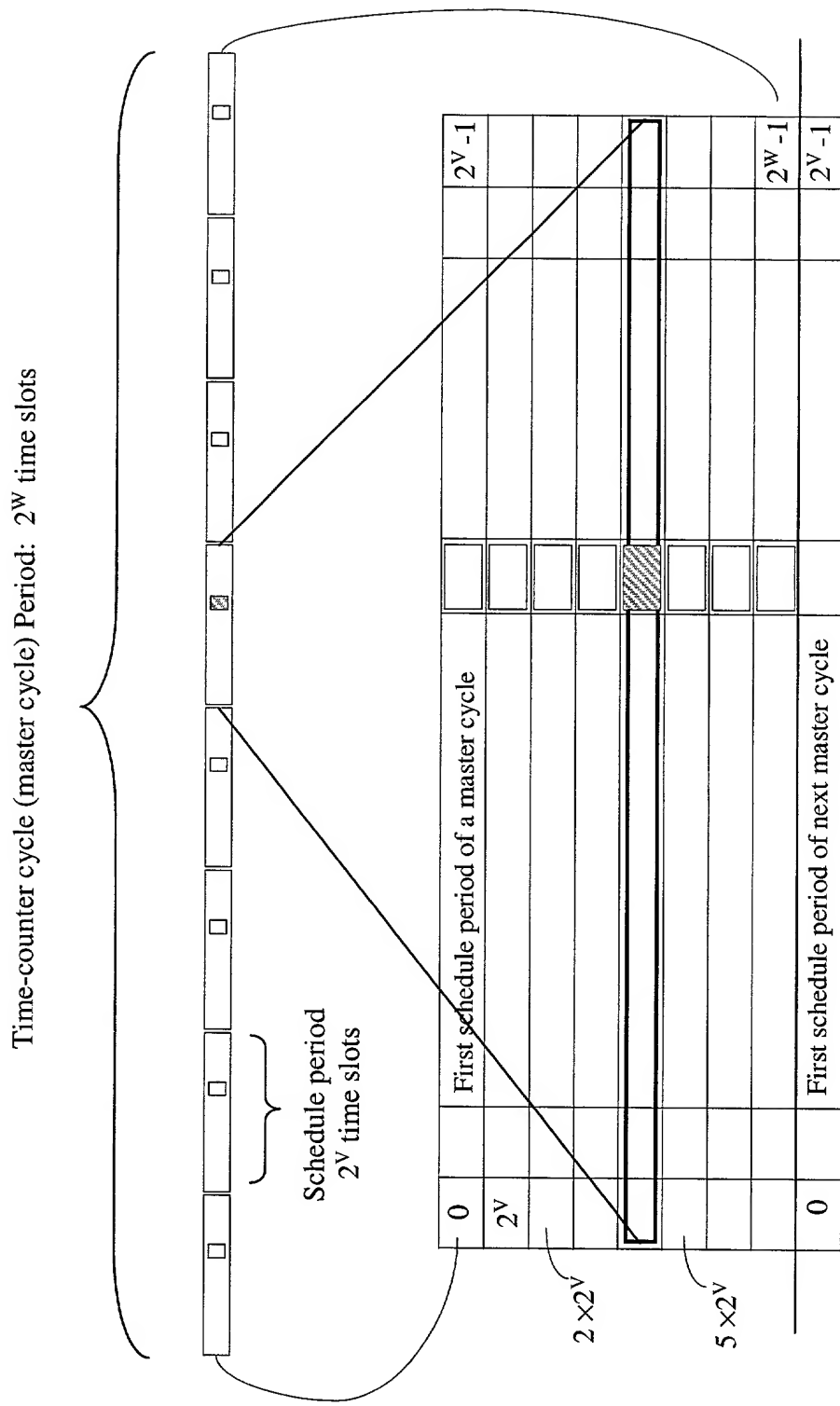


FIG. 19

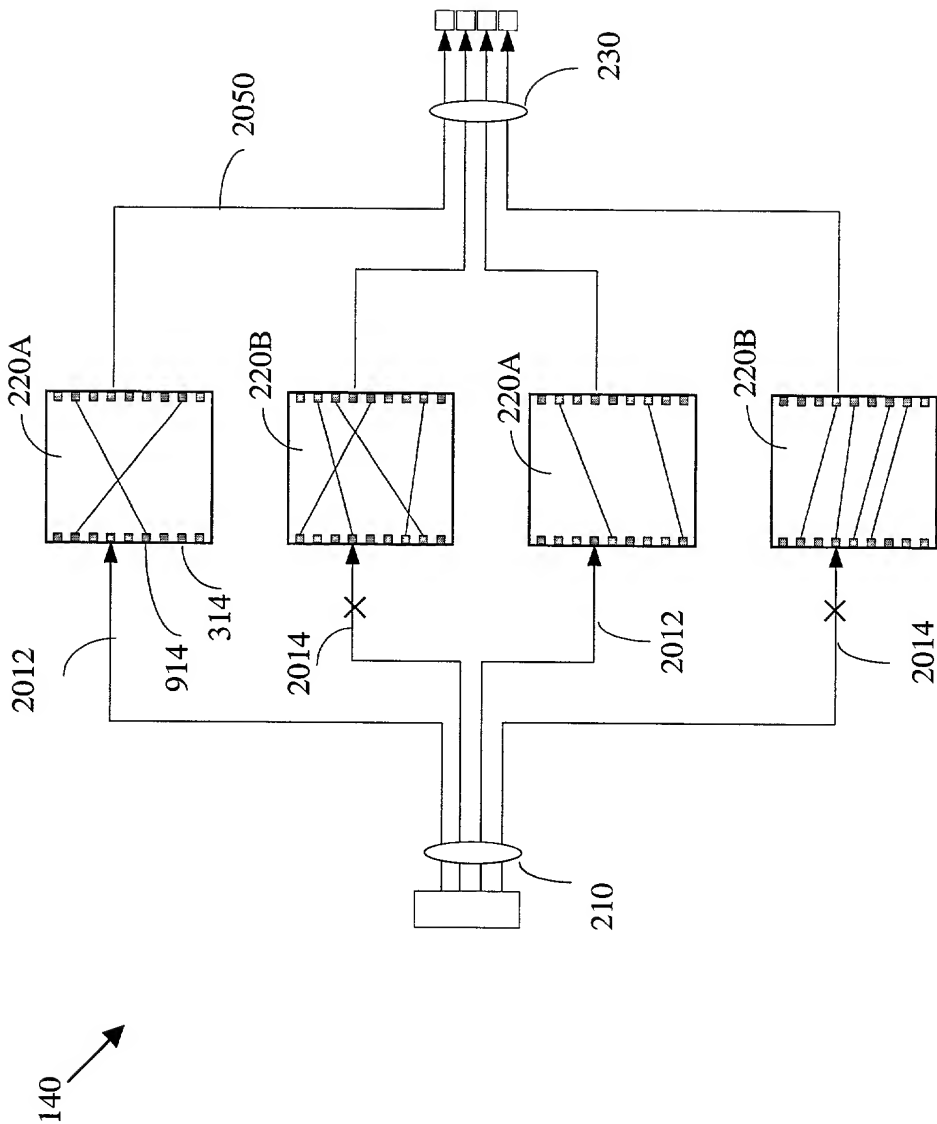


FIG. 20

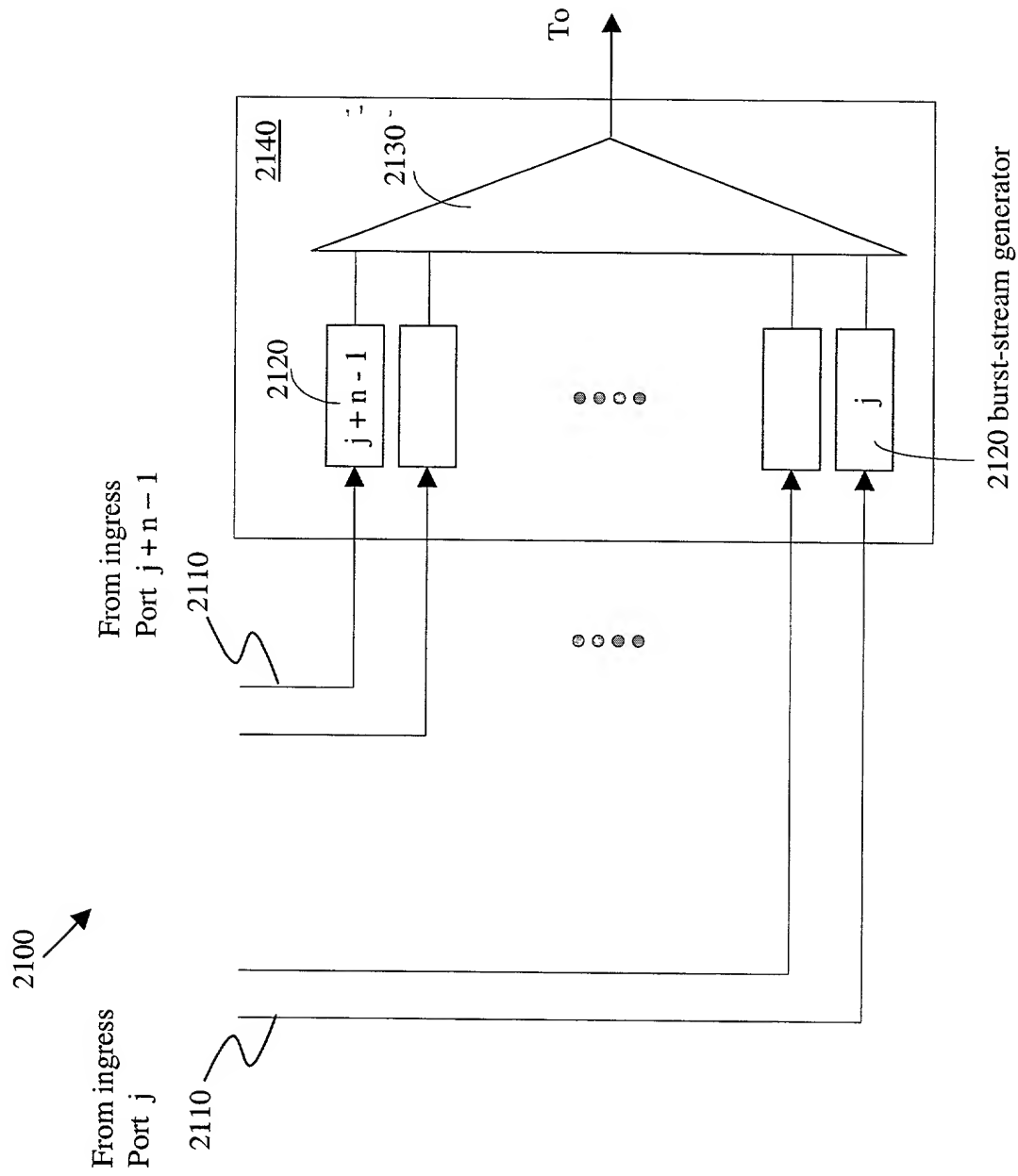


FIG. 21

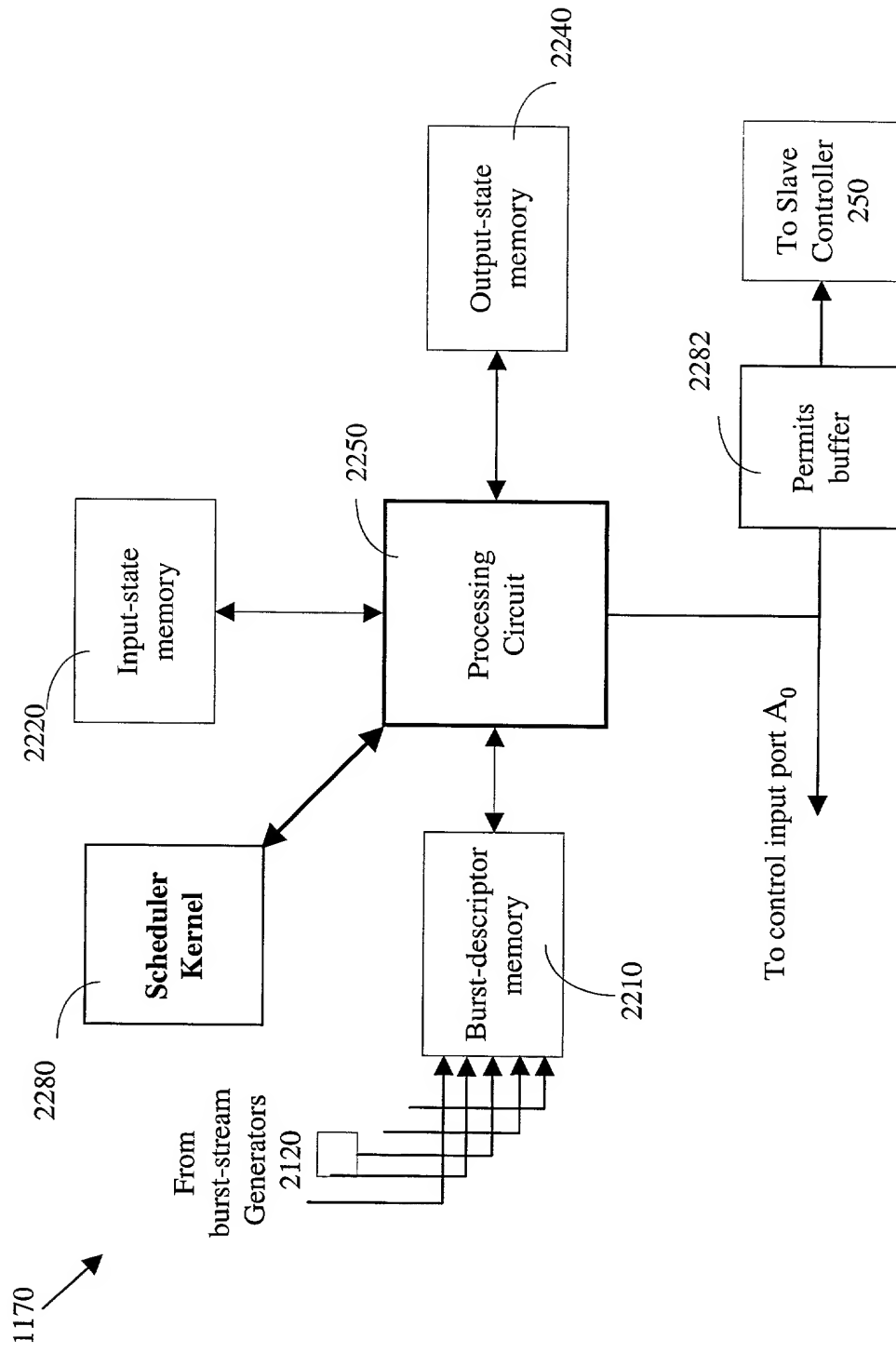


FIG. 22

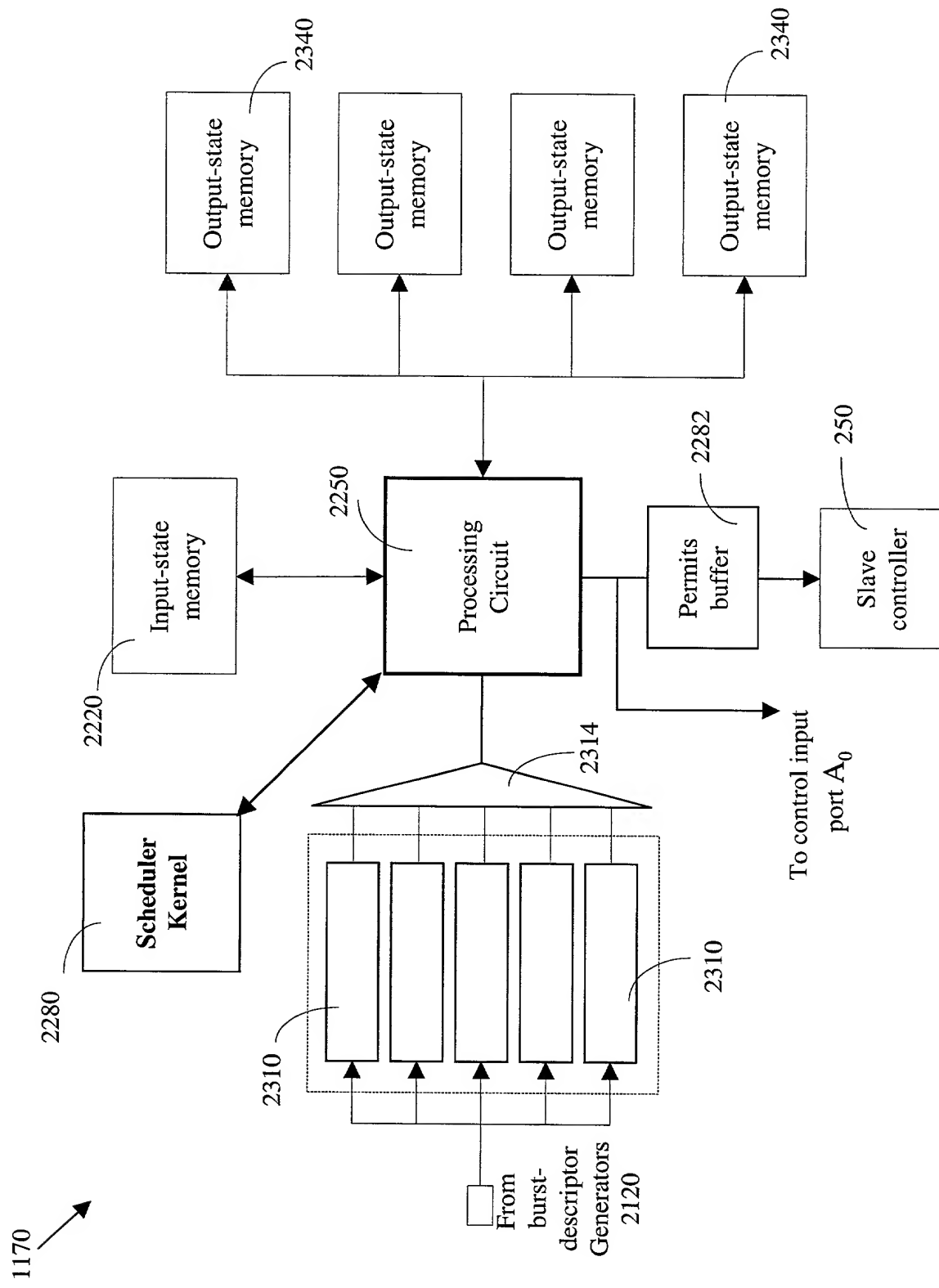


FIG. 23

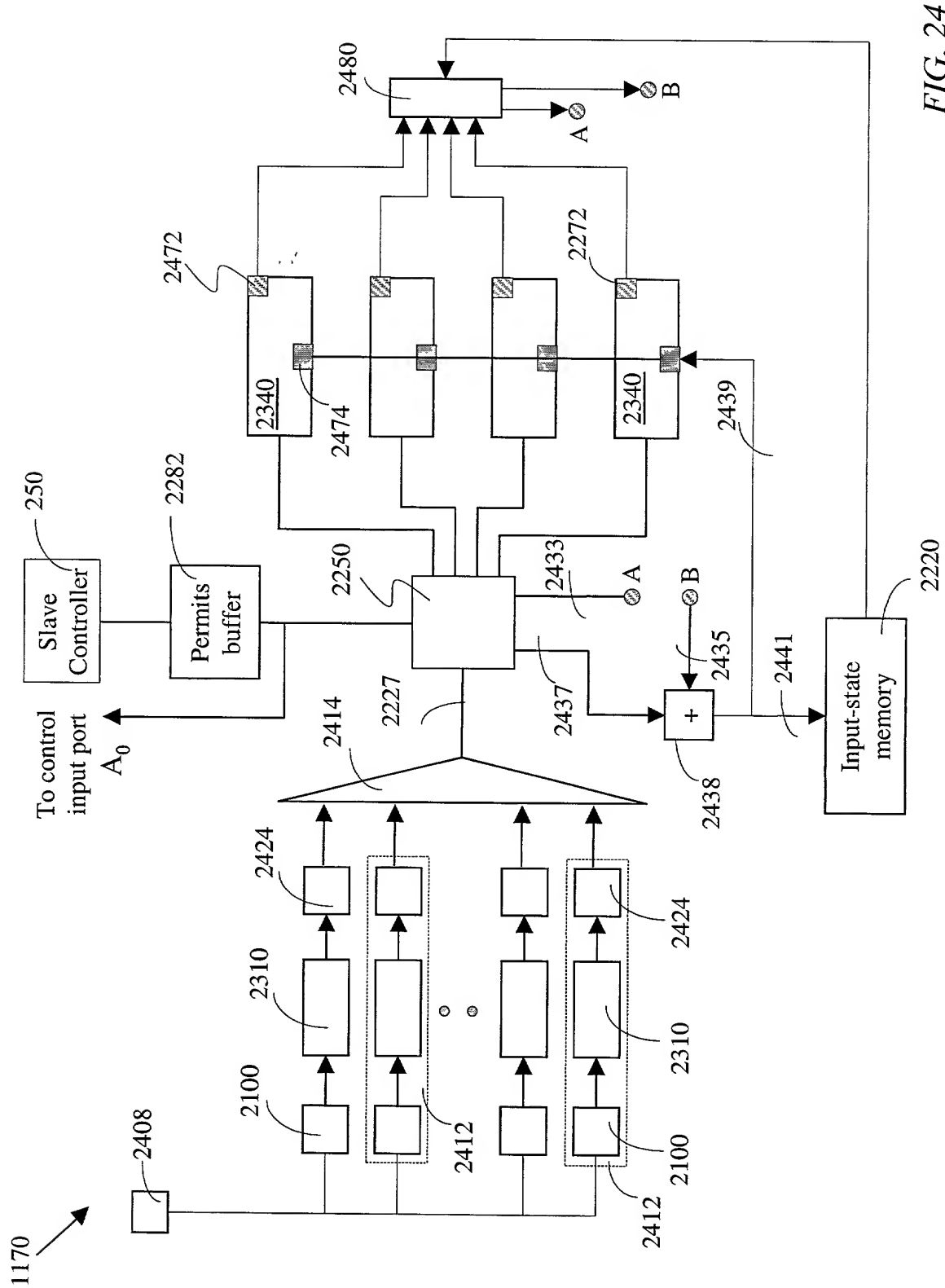


FIG. 24

Input port															
1	20122	2520													
2	23128														
3	24282	2522													
4	18892														
5	23000														
6	18000														
7	20908														
8	18421	X													
9	20584														
10	22508														
11	24812	2510													
12	20080														
13	21888														
14	24120														
15	19987														
16	20585														
Output port															
1	20585	2540													
2	18892														
3	23000	2542													
4	24120														
5	18520	X													
6	19987														
7	20080														
8	24282														
9	24812	2580													
10	20122														
11	20584														
12	20908														
13	18000														
14	21888														
15	22508														
16	23128														

FIG. 25

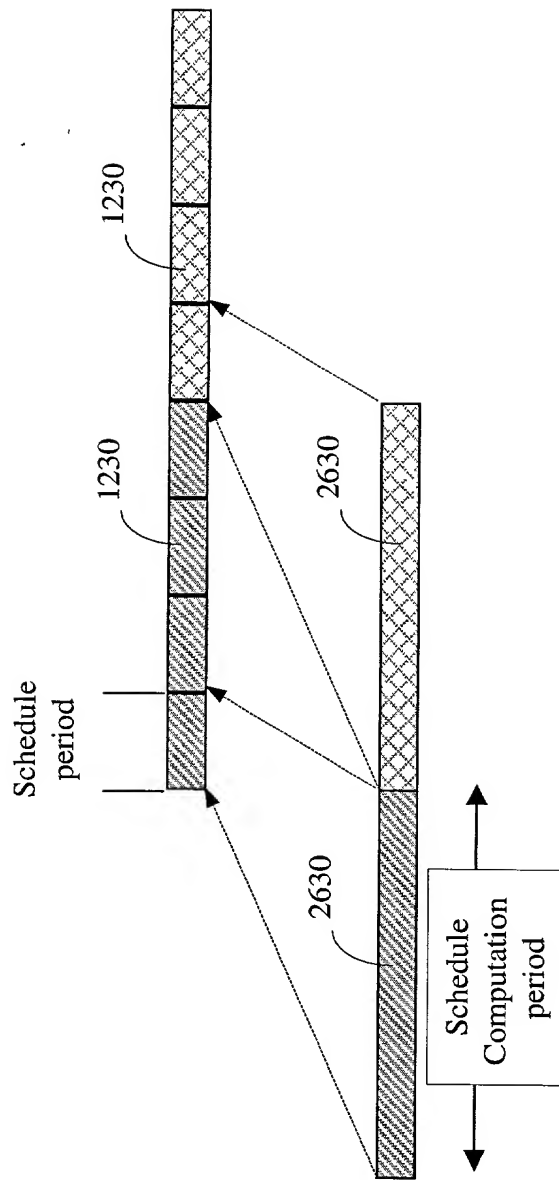


FIG. 26

FIG. 27

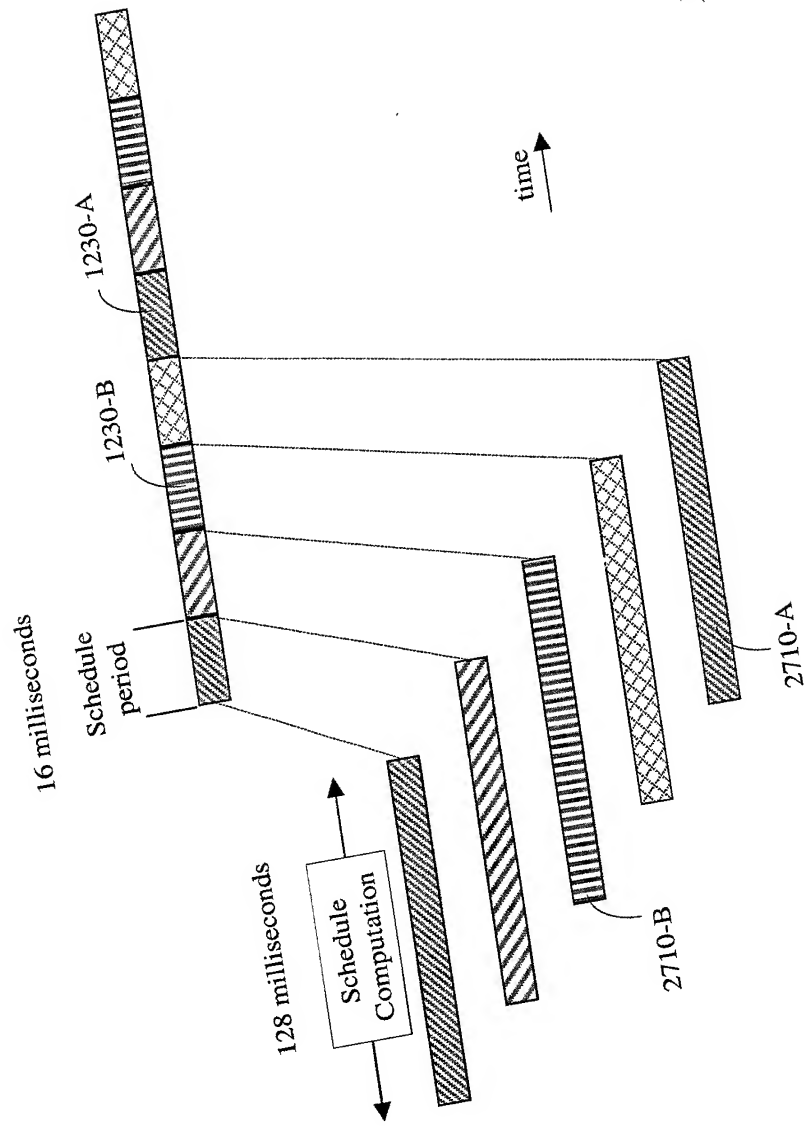


FIG. 27

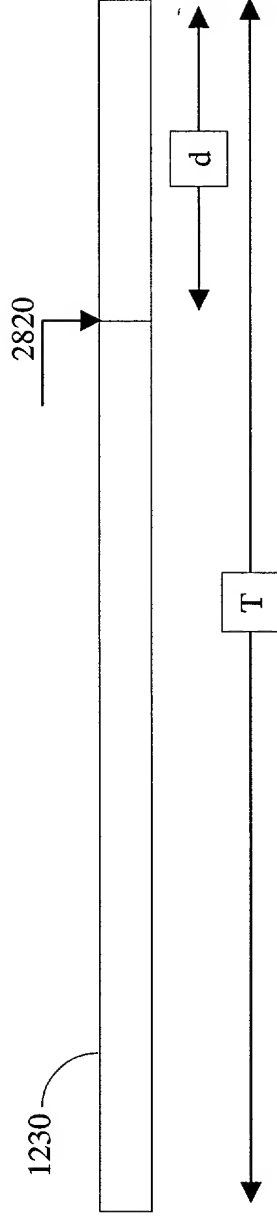


FIG. 28-a

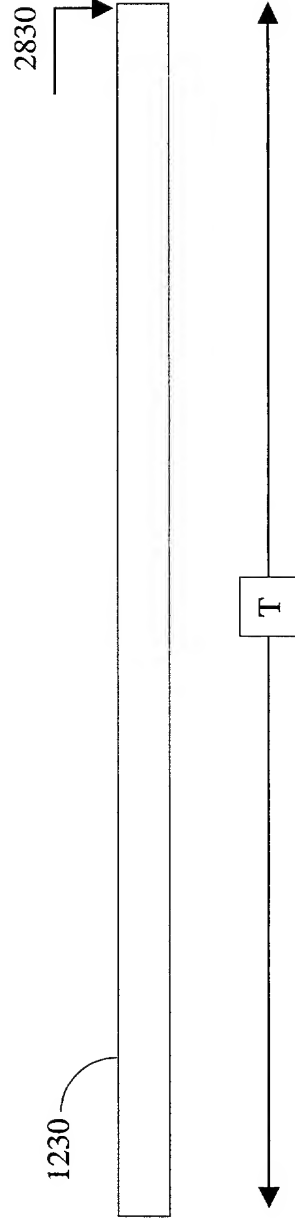


FIG. 28-b

FIG. 28

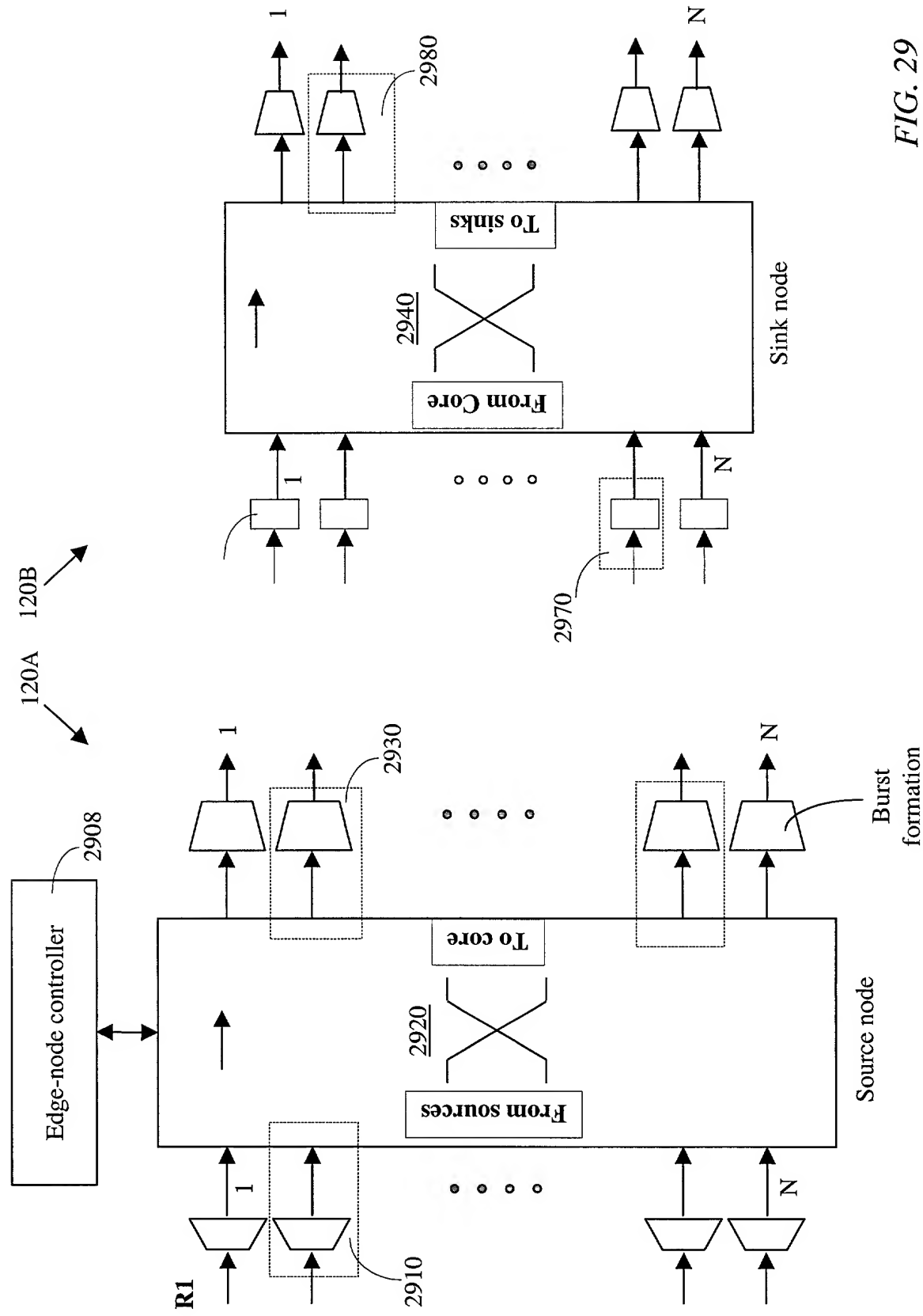


FIG. 29

120 ↗

120A →

120B →

From sources

From Core

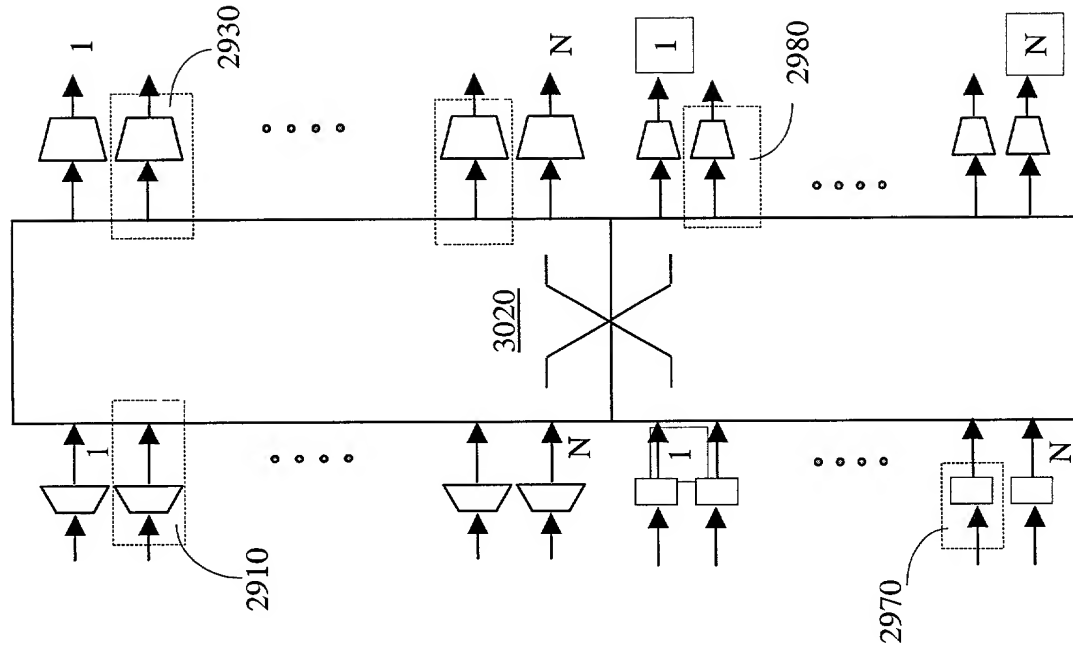


FIG. 30

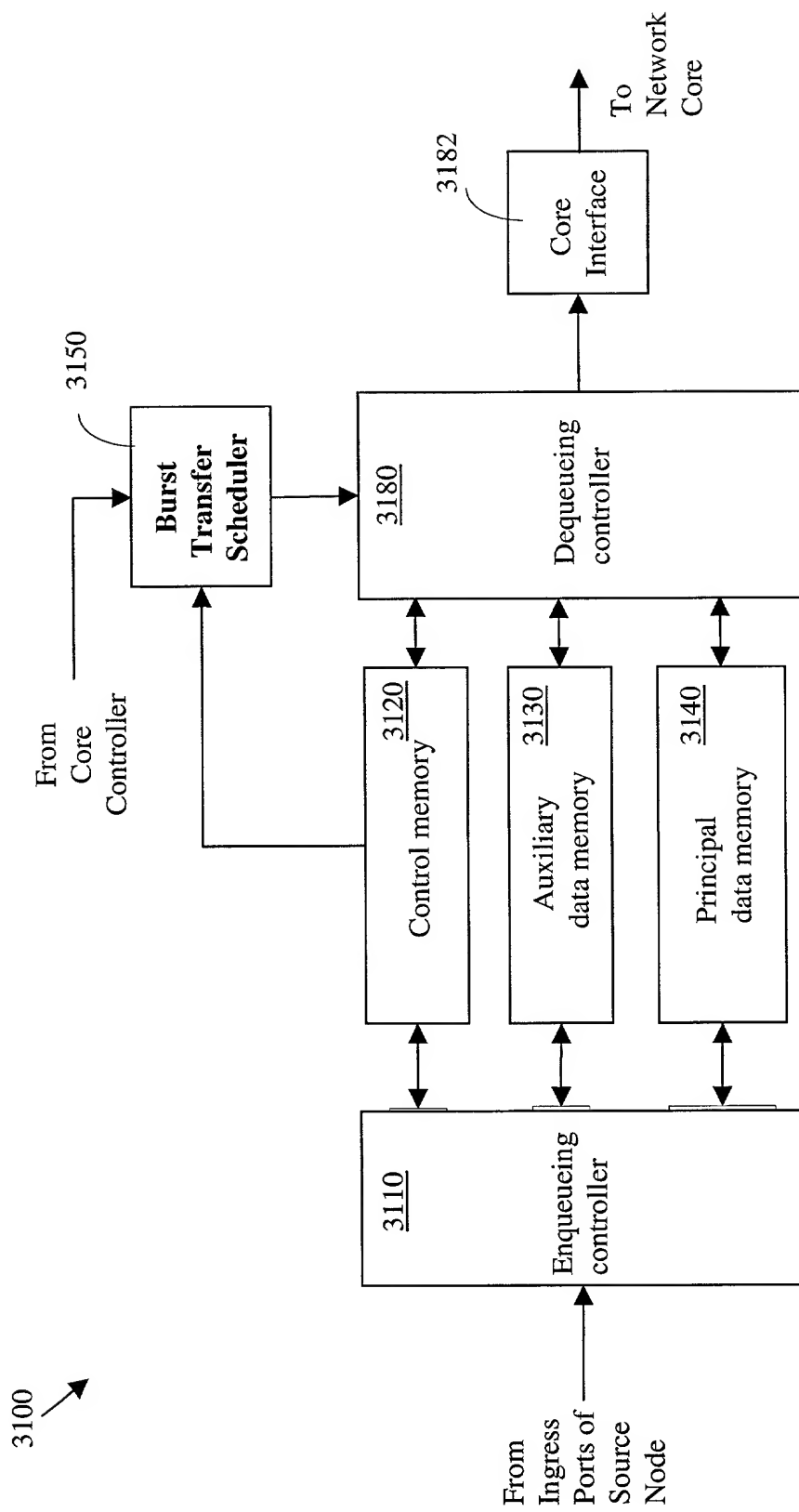


FIG. 31

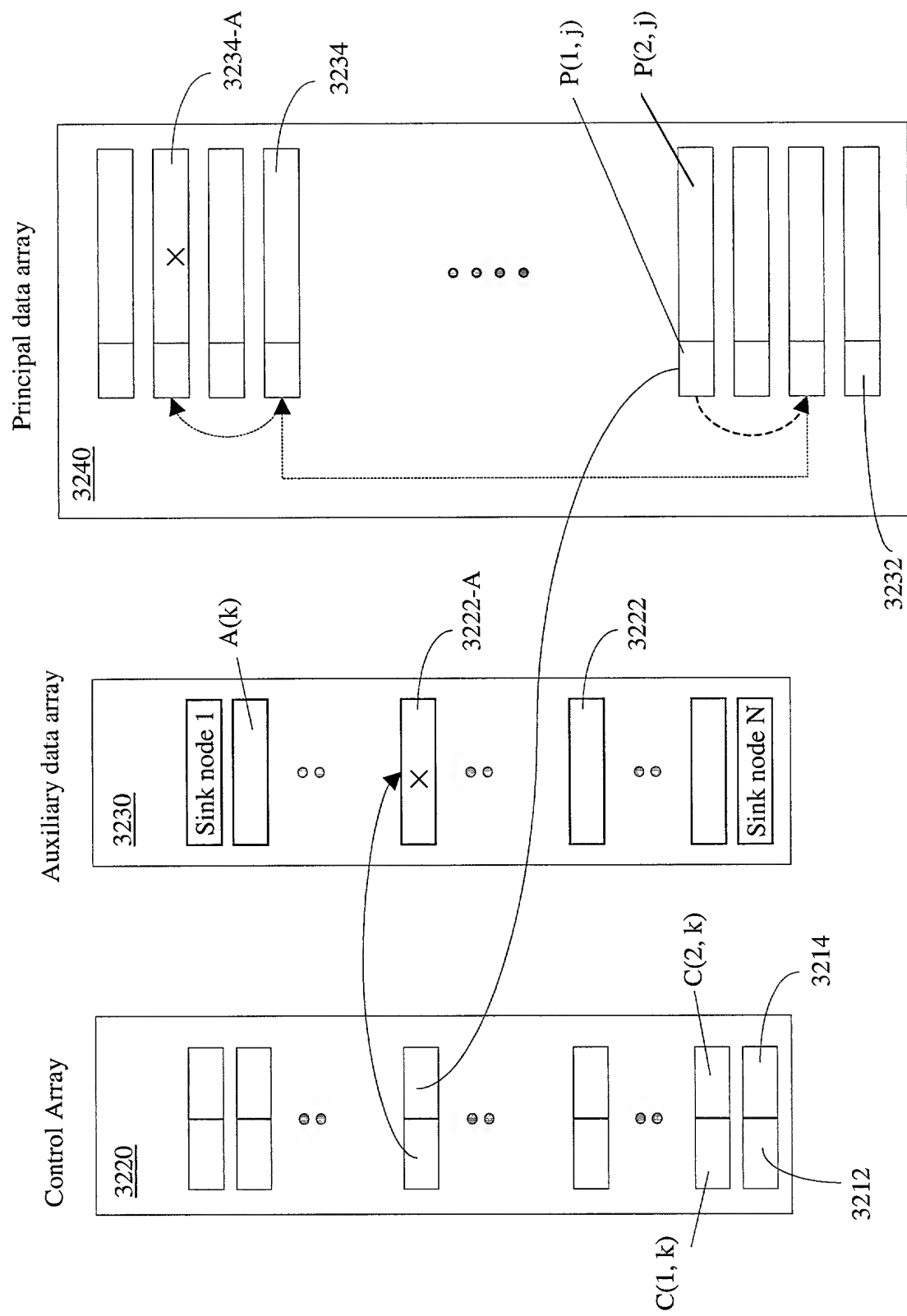


FIG. 32

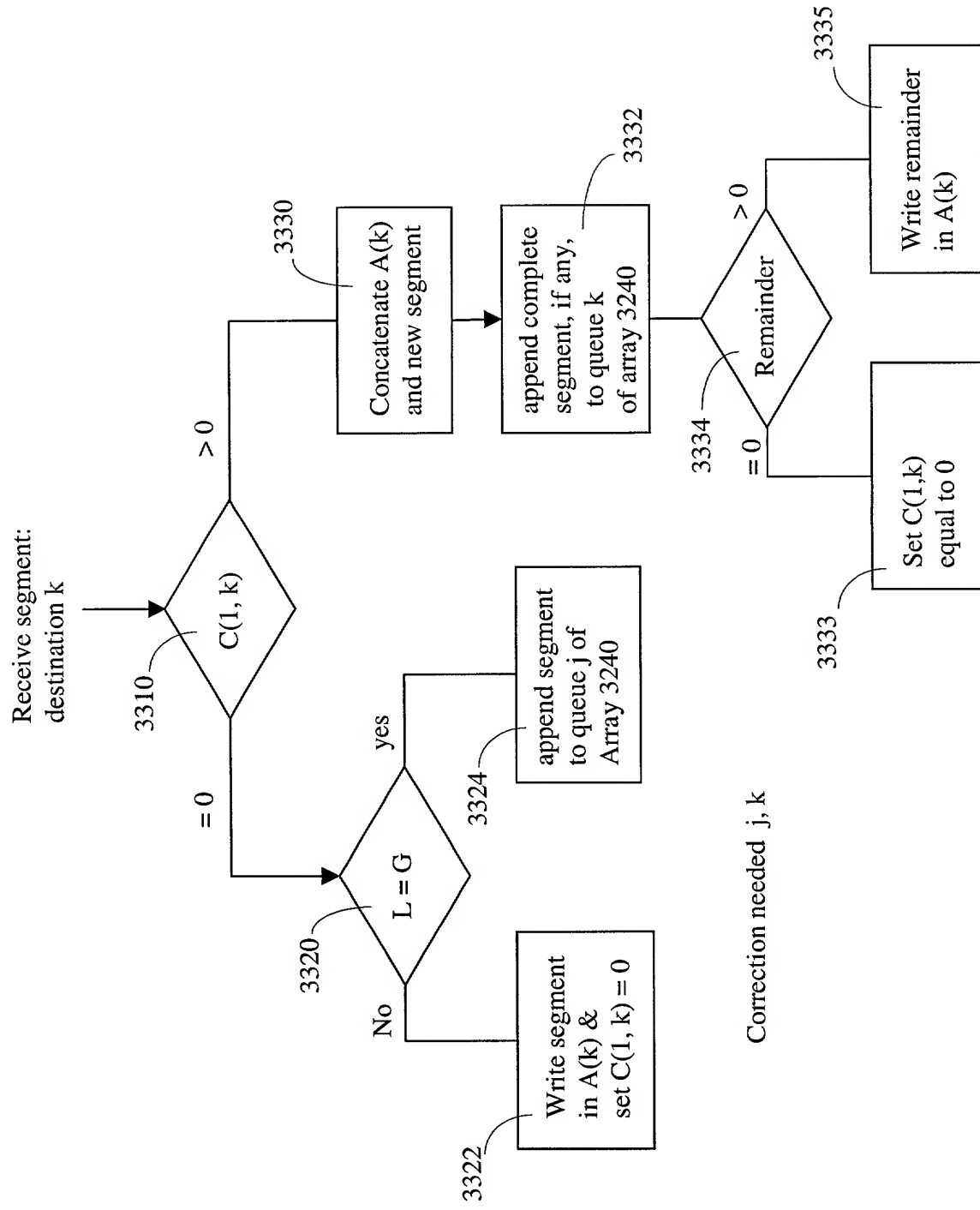


FIG. 33

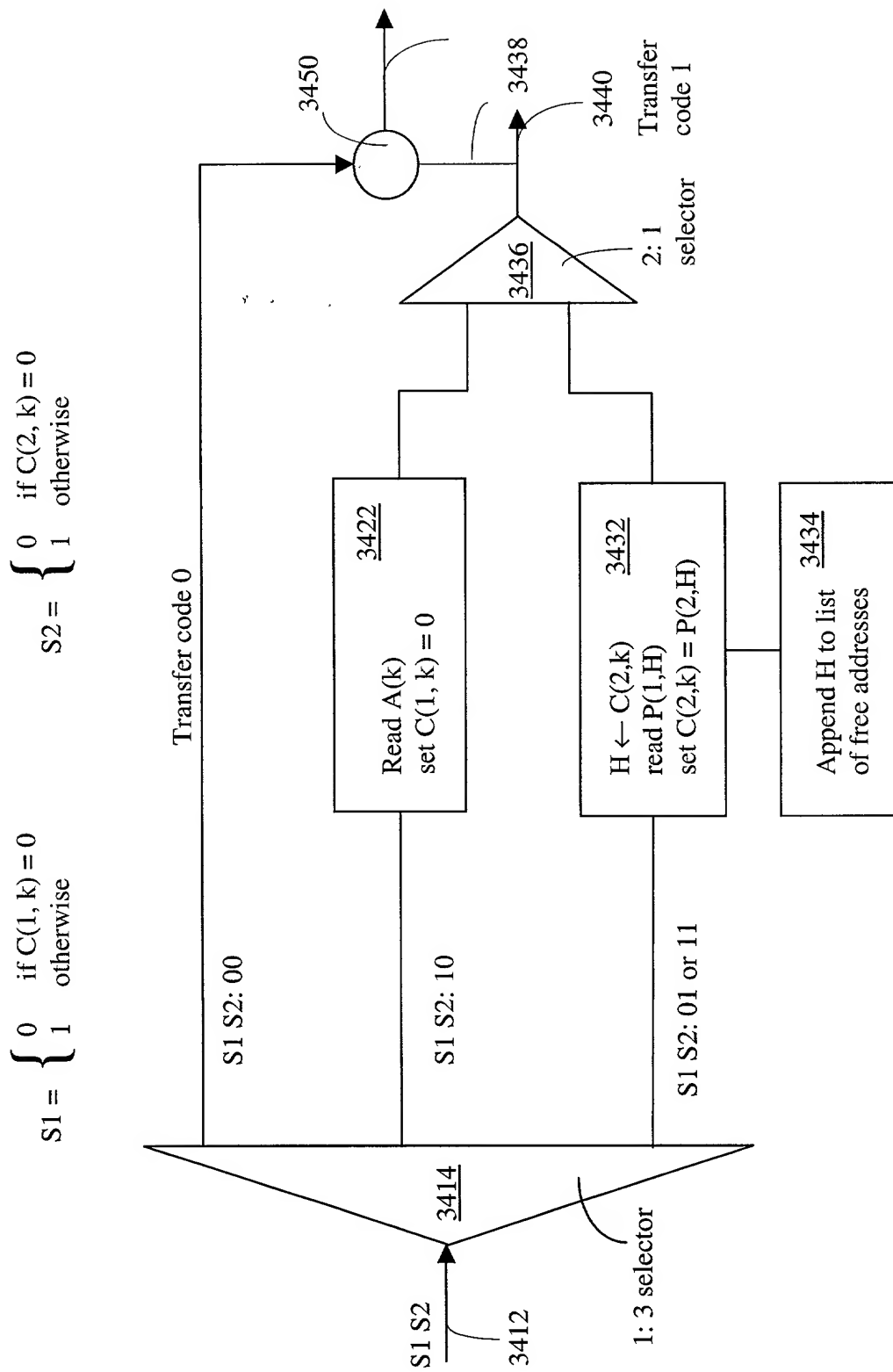


FIG. 34

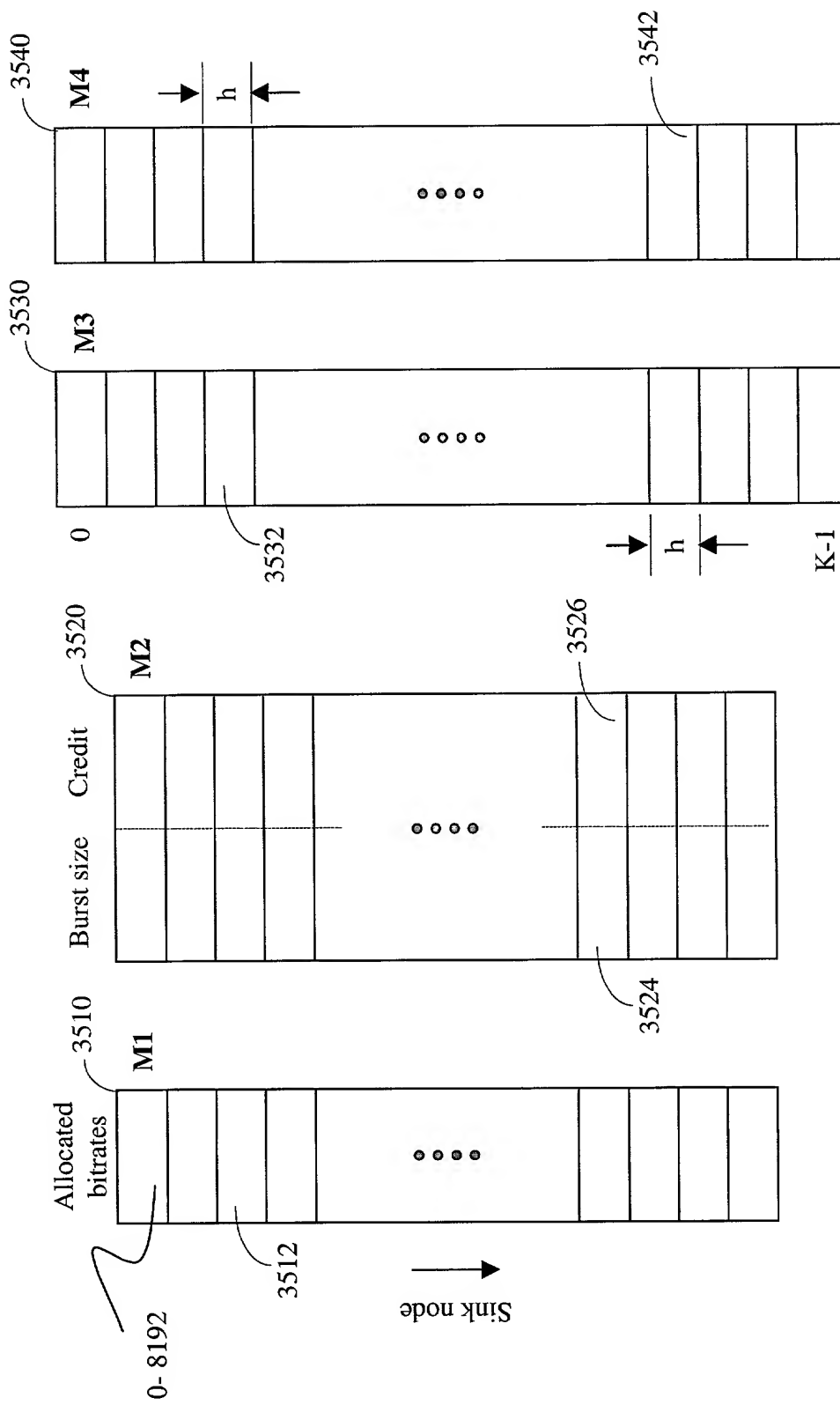


FIG. 35

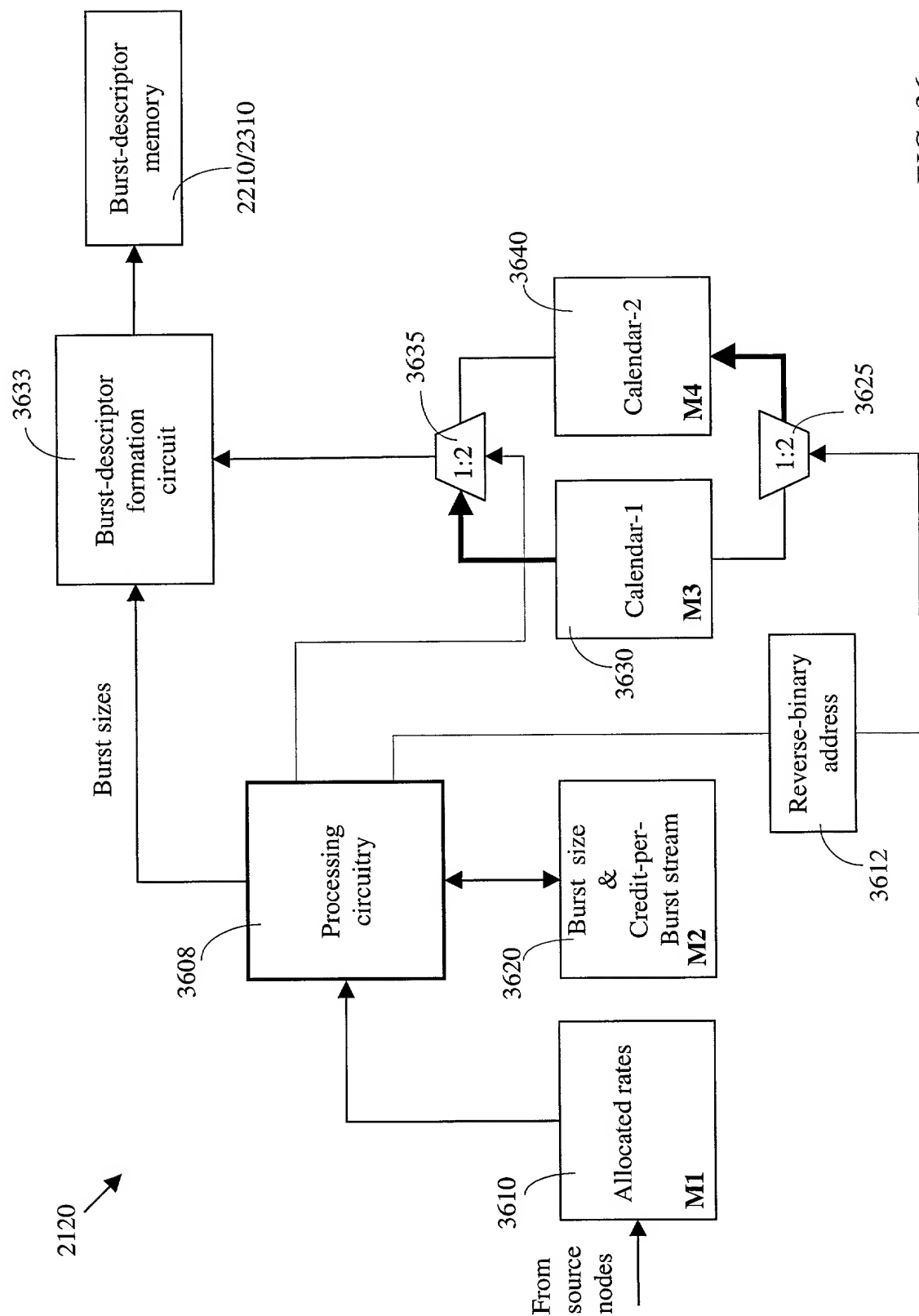


FIG. 36